Manoj Franklin

Electrical Engineering Department, and
University of Maryland Institute for Advanced Computer Studies (UMIACS)
University of Maryland
1417 A.V. Williams Building
College Park, MD 20742-3285
Email: manoj@eng.umd.edu
Ph: (301) 405-6712 Fax: (301) 314-9281

OBJECTIVE

To become an excellent researcher and educator at University of Maryland, College Park. My primary interests are with Computer Architecture, in particular Instruction-Level Parallel (ILP) Processing, Microarchitecture, and ILP compilation.

EDUCATION

Ph.D.:	Computer Sciences University of Wisconsin-Madison, 1993 Cumulative GPA: 4.0 on a 4.0 scale. Thesis: The Multiscalar Architecture
M.S.:	Computer Sciences University of Wisconsin-Madison, 1990 Cumulative GPA: 4.0 on a 4.0 scale. Thesis: Row/Column Pattern Sensitive Faults in Random Access Memories
B.Sc. (Engg):	Electronics and Communications Engineering University of Kerala, India, 1984.

WORK EXPERIENCE

Electrical and Computer Engineering Department, University of Maryland, College Park
Assistant Professor (August 1998 - Present)

Electrical and Computer Engineering Department, Clemson University
Assistant Professor (September 1993 - August 1998)

IBM Graduate Fellow (September 1990 - May 1993)

IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA
Intern (Summer 1991, November 1991 - December 1991)

Cray Research, Inc., Chippewa Falls, WI 54729, USA
Summer Intern (Summer 1990)

Computer Sciences Department, University of Wisconsin-Madison
Research Assistant (Spring 1990, Summer 1992, Summer 1993)

Computer Sciences Department, University of Wisconsin-Madison
Teaching Assistant (January 1988 - December 1989)
TA for Machine Organization and Basic Systems, and Algebraic Language Programming.

Space Science and Engineering Center, University of Wisconsin-Madison
Software development (Fall 1987 and Summer 1988)

Developed software for receiving pictures from satellites, and test routines for digital systems.

Electronics Division, Bharat Heavy Electricals Ltd., Bangalore, India
Engineer (September 1984 - August 1987)
Developed the control system for the first HVDC project in India.

ACADEMIC HONORS

Clemson University Board of Trustees 1997 Faculty Excellence Award.
NSF CAREER (Faculty Early Career Development) Award, 1997-2001.
NSF Research Initiation Award, 1994-1997.
Ph.D. thesis featured in *Microprocessor Report*, October 2, 1995.
Ph.D. thesis nominated by University of Wisconsin for ACM Dissertator Award.
IBM Graduate Fellowship, 1990-93.
Nominated for Best Paper Award in VLSI Design '94.
National Merit Scholarship, India, 1977.
Kerala State Merit Scholarship, India, 1977.

PUBLICATIONS (JOURNALS and REFEREED CONFERENCES)

[1] M. Franklin, K. K. Saluja, and K. Kinoshita, "Row/Column Pattern Sensitive Fault Detection in RAMs via Built-In Self-Test," *Proc. International Symposium on Fault-Tolerant Computing (FTCS-19)*, pp. 36-43, June 1989.

[2] G. S. Sohi, M. Franklin, and K. K. Saluja, "A Study of Time-Redundant Fault Tolerance Techniques for High-Performance Pipelined Computers," *Proc. International Symposium on Fault-Tolerant Computing (FTCS-19)*, pp. 436-443, June 1989.

[3] M. Franklin, K. K. Saluja, and K. Kinoshita, "Design of a BISTRAM with Row/Column Pattern Sensitive Fault Detection Capability," *Proc. International Test Conference (ITC)*, pp. 327-336, August 1989.

[4] M. Franklin, K. K. Saluja, and K. Kinoshita, "A Built-In Self-Test Algorithm for Row/Column Pattern Sensitive Faults in RAMs," *IEEE Journal of Solid-State Circuits*, Vol. 25, pp. 514-524, April 1990.

[5] M. Franklin and K. K. Saluja, "Built-In Self-Testing of Random Access Memories," *IEEE Computer*, pp. 45-56, October 1990.

[6] G. S. Sohi and M. Franklin, "High-Bandwidth Data Memory Systems for Superscalar Processors," *Proc. Architectural Support for Programming Languages and Operating Systems (ASPLOS-IV)*, pp. 53-62, 1991.

[7] M. Franklin and K. K. Saluja, "Pattern Sensitive Fault Testing of RAMs with Built-In ECC," *Proc. International Symposium on Fault-Tolerant Computing (FTCS-21)*, pp. 385-392, June 1991.

[8] M. Franklin and K. K. Saluja, "An Algorithm to Test RAMs for Physical Neighborhood Pattern Sensitive Faults," *Proc. International Test Conference (ITC)*, pp. 675-684, 1991.

[9] M. Franklin and G. S. Sohi, "A New Paradigm for Exploiting Fine-Grain Parallelism," *Proc. 25th Hawaii International Conference on System Sciences (HICSS-25) Volume 1*, pp. 4-13, 1992.

[10] P. Ramanathan, K. K. Saluja, and M. Franklin, "Zero Cost Testing of Check Bits in RAMs with On-Chip ECC," *Proc. 10th IEEE VLSI Test Symposium*, April 1992.

[11] M. Franklin and G. S. Sohi, "The Expandable Split Window Paradigm for Exploiting Fine-Grain Parallelism," *Proc. 19th Annual International Symposium on Computer Architecture (ISCA)*, pp.58-67, 1992.

[12] M. Franklin and G. S. Sohi, "Register Traffic Analysis for Streamlining Inter-Operation Communication in Fine-Grain Parallel Processors," *Proc. The 25th Annual International Symposium on Microarchitecture (MICRO-25)*, pp. 236-245, 1992.

[13] P. Ramanathan, K. K. Saluja, and M. Franklin, "Testing Check Bits at No Cost in RAMs with On-Chip ECC," *Proc. IEE (Part E)*, Vol. 140, No. 6, pp. 304-306, November 1993.

[14] B. Narendran, M. Franklin, and K. K. Saluja, "Parallel Computation of LFSR Signatures," *Proc. 2nd Asian Test Conference (ATS)*, 1993.

[15] D. Pnevmatikatos, M. Franklin, and G. S. Sohi, ''Control Flow Prediction for Dynamic ILP Processors,'' *Proc. 26th Annual International Symposium on Microarchitecture (MICRO-26)*, pp. 153-163, 1993.

[16] M. Franklin and K. K. Saluja ''An Algorithm to Test Reconfigured RAMs,'' *Proc. 7th International Conference on VLSI Design (VLSI Design '94)*, 1994.

[17] M. Franklin and K. K. Saluja, "Hypergraph Coloring and Reconfigured RAM Testing," *IEEE Transactions on Computers*, Vol. 43, pp. 725-736, June 1994.

[18] M. Franklin and K. K. Saluja, "Theory and Techniques for Testing Check-Bits of RAMs with On-Chip ECC," *IEICE (Institute of Electronics, Information and Communication Engineers) Transactions on Information and Systems*, Vol. E76-D, No. 10, pp. 1243-1252, October 1993.

[19] M. Franklin and M. Smotherman, ''A Fill-Unit Approach to Multiple Instruction Issue,'' *Proc. 27th International Symposium on Microarchitecture (MICRO-27)*, pp. 162-171, 1994.

[20] M. Franklin, K. K. Saluja, and K. Kim, ''Fast Computation of MISR Signatures,'' *Proc. 8th International Conference on VLSI Design (VLSI Design '95)*, pp. 414-418, 1995.

[21] S. Dutta and M. Franklin, ''Block-Level Prediction for Wide-Issue Superscalar Processors,'' *Proc. 1st International Conference on Algorithms and Architectures for Parallel Processing*, Vol. 1, pp. 143-152, 1995.

[24] M. Franklin, ''Incorporating Fault Tolerance in the Multiscalar Fine-Grain Parallel Processor,'' *Proc. International Conference on Parallel Processing (ICPP)*, Vol. I, pp. 110-117, 1995.

[25] M. Franklin, ''A Study of Time Redundant Fault Tolerance Techniques for Superscalar Processors,'' *Proc. IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems (DFT '95)*, pp. 207-215, 1995.

[26] M. Franklin, ''Fast Computation of C-MISR Signatures,'' *Proc. 4th Asian Test Symposium*, pp. 293-297, 1995.

[27] M. Smotherman and M. Franklin, ''Improving CISC Instruction Decoding Performance Using a Fill Unit,'' *Proc. International Symposium on Microarchitecture (MICRO-28)*, 1995.

[28] S. Dutta and M. Franklin, ''Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors,'' *Proc. International Symposium on Microarchitecture (MICRO-28)*, pp. 258-263, 1995.

[29] M. Franklin, ''Multi-Version Caches for Multiscalar Processors,'' *Proc. International Conference on High Performance Computing*, pp. 99-104, 1995.

[30] M. Franklin and G. S. Sohi, "ARB: A Hardware Mechanism for Dynamic Memory Disambiguation," *IEEE Transactions on Computers*, Vol. 45, No. 5, pp. 552-571, May 1996.

[31] G. A. Kemp and M. Franklin, ''PEWs: A Decentralized Dynamic Scheduler for ILP Processing,'' *Proc. International Conference on Parallel Processing (ICPP)*, Vol. I, pp. 239-246, 1996.

[32] M. Franklin and K. K. Saluja, ''An Algorithm to Test Reconfigured RAMs for Pattern Sensitive Faults,'' *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 9, pp. 1081-1087, September 1996.

[33] M. Franklin, ''Incorporating Fault Tolerance in Superscalar Processors,'' *Proc. 3rd International Conference on High Performance Computing*, pp. 301-306, 1996.

[34] V. K. Madavarapu, M. Franklin, and K. K. Sundararaman, ''A Study of Dynamic Scheduling Techniques for Multiscalar Processors,'' *Proc. 3rd International Conference on High Performance Computing*, pp. 413-418, 1996.

[35] K. K. Sundararaman and M. Franklin, ''Multiscalar Execution along a Single Flow of Control,'' *Proc. International Conference on Parallel Processing (ICPP), pp. 106-113, 1997.*

[36] K. Wang and M. Franklin, ''Highly Accurate Data Value Prediction using Hybrid Predictors,'' *Proc. International Symposium on Microarchitecture (MICRO-30)*, pp. 281-290, 1997.

[37] B. Cyril and M. Franklin, ''A Study of Tree-Based Control Flow Prediction Schemes,'' *Proc. International Conference on High Performance Computing (HiPC)*, pp. 28-33, 1997.

[38] K. Wang and M. Franklin, ''Highly Accurate Data Value Prediction,'' *Proc. International Conference on High Performance Computing (HiPC)*, pp. 358-363, 1997.

[39] R. Sathe, K. Wang, and M. Franklin, ‘‘Techniques for Performing Highly Accurate Data Value Prediction,’’ *Microprocessors and Microsystems*, Vol. 22, No. 6, pp. 303-313, 30 November 1998.

[40] N. Ranganathan and M. Franklin, ‘‘The PEWs Microarchitecture: Reducing Complexity Through Data Dependence based Decentralization,’’ *Microprocessors and Microsystems*, Vol. 22, No. 6, pp. 333-343, 30 November 1998.

[41] N. Ranganathan and M. Franklin, ‘‘An Empirical Study of Decentralized ILP Execution Models,’’ *Proc. 8th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VIII)*, pp. 272-281, 1998.

[42] R. Sathe and M. Franklin, ‘‘Available Parallelism with Data Value Prediction,’’ *Proc. International Conference on High Performance Computing (HiPC)*, pp. 194-201, 1998.

[43] B. R. Toone and M. Franklin, ‘‘Control Flow Prediction with Unbalanced Tree-like Subgraphs,’’ *Proc. International Conference on High Performance Computing (HiPC)*, pp. 221-227, 1998.

[44] S. Dutta and M. Franklin, ‘‘Control Flow Prediction Schemes for Wide-Issue Superscalar Processors,’’ (to appear in) *IEEE Transactions on Parallel and Distributed Systems*.

PUBLICATIONS (INVITED)

[1] M. Franklin and K. K. Saluja, ‘‘Embedded RAM Testing,’’ *IEEE International Workshop on Memory Technology, Design and Testing*, 1995.

PUBLICATIONS (TECHNICAL REPORTS)

[1] M. Franklin, K. K. Saluja, and K. Kinoshita, “An Algorithm for the Detection of Row/Column Pattern Sensitive Faults in RAMs,” Technical Report ECE-89-5, Dept. of Electrical and Computer Engineering, University of Wisconsin-Madison, April 1989.

[2] M. Franklin, “Row/Column Pattern Sensitive Faults in Random Access Memories,” M.S. Thesis, Computer Sciences Department, University of Wisconsin-Madison, 1990.

[3] G. S. Sohi and M. Franklin, “High-Bandwidth Data Memory Systems for Superscalar Processors,” Technical Report TR 968, Computer Sciences Department, University of Wisconsin-Madison, Sept. 1990.

[4] M. Franklin and K. K. Saluja, “Theory and Techniques for Testing RAMs with Built-In ECC,” Technical Report ECE-91-5, Dept. of Electrical and Computer Engineering, University of Wisconsin-Madison, March 1991.

[5] P. Ramanathan, K. K. Saluja, and M. Franklin, “Low Cost Testing of Check Bits in RAMs with ECC,” Technical Report ECE-92-1, Dept. of Electrical and Computer Engineering, University of Wisconsin-Madison, January 1992.

[6] N. Ranganathan and M. Franklin, ‘‘Complexity-Effective PEWs Microarchitecture,’’ Technical Report, Dept. of Electrical and Computer Engineering, Clemson University, November 1997.

RESEARCH GRANTS AWARDED

NSF Research Initiation Award: Incorporating Fault Tolerance in the Multiscalar Processor, 1994-1997, $99,978.

NSF Research Experience for Undergraduates, Summer 1997 (Co-PI).

NSF CAREER (Faculty Early Career Development) Award: Transcending the Limits to ILP Processing, 1997-2001, $200,000.

NSF: Exploring Multiple Control Flows for ILP Processors, 1997-1999, $129,712.

NSF: CISE Infrastructure Award, 1998, $60,994.

JOURNALS / CONFERENCES REVIEWED FOR

[1] IEEE Transactions on Computers
[2] IEEE Transactions on Parallel and Distributed Systems
[3] IEEE Computer
[4] IEEE Design & Test of Computers
[5] Journal of Supercomputing
[6] Journal of Parallel and Distributed Computing
[7] Performance Evaluation Journal (Special issue on Performance Modeling of Parallel Processing Systems)
[8] International Symposium on Computer Architecture (ISCA)
[9] International Symposium on Fault-Tolerant Computing (FTCS)
[10] International Test Conference (ITC)
[11] MICRO-25, MICRO-27, MICRO-28
[12] IEEE Symposium on Parallel and Distributed Processing (SPDP '93)
[13] International Symposium on High-Performance Computer Architecture (HPCA-2)
[14] IEEE VLSI Test Symposium

OTHER PROFESSIONAL ACTIVITIES

[1] Session chair for Asian Test Symposium (ATS '95)
[2] Session chair for 27th International Conference on Parallel Processing (ICPP), 1997
[3] Registration chair for 30th International Symposium on Microarchitecture
[4] Program Committee Member for 31st International Symposium on Microarchitecture
[5] Program Committee Member for Workshop on Workload Characterization
[6] Program Committee Member for 1999 International Conference on Computer Design