1. Explain why we need a memory hierarchy.

2. Consider a computer system that has a cache with 512 blocks, each of which can store 32 bytes. Which cache set will the memory address 0xFBFC map to:
   (i) if it is a direct-mapped cache
   (ii) if it is an 8-way set-associative cache
   (iii) if it is a fully-associative cache.

3. The CPU in your computer produces 22-bit addresses, with each addressable item being 1 byte. The computer has 16K bytes of physical memory. The page size is 4 Kbytes. (i) How many bits of the 22-bit address are used to determine the page offset? 
   (ii) How many virtual pages exist? 
   (iii) How many physical pages exist? 
   (iv) How many entries will the page table have?

4. In order to improve the memory access time from 10 cycles, the system designer decided to incorporate a cache memory, which has an access time of 1 cycle. The cache was able to supply data for 90% of the memory references. Has the cache memory improved the memory system’s performance or decreased it?

5. Some people have argued that with increasing capacity of memory storage per chip, cache memory is an idea whose time has passed, and they expect to see it dropped from future computers. Find reasons for and against this argument.

6. Consider the following DLX code:

   LOOP:  LD     F0, 0(R1)  
          ADDD   F0, F0, F4  
          MULT   F0, F0, F2  
          SD     0(R1), F0  
          SUBI   R1, R1, 8  
          BNEZ   R1, LOOP  
          NOP

   Assume the standard DLX pipeline, with data forwarding. The integer unit takes a single cycle for execution. The floating point adder/subtractor/multiplier(s) are pipelined, and have 3 stages. Perform software pipelining of this code so as to schedule it in a multiple-issue processor.
   **Show both prolog and epilog.**