Homework 6 Solution

ENEE 303

Spring 2019

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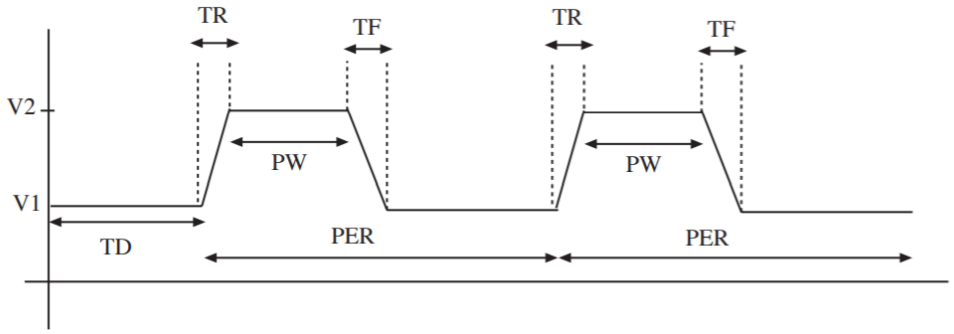
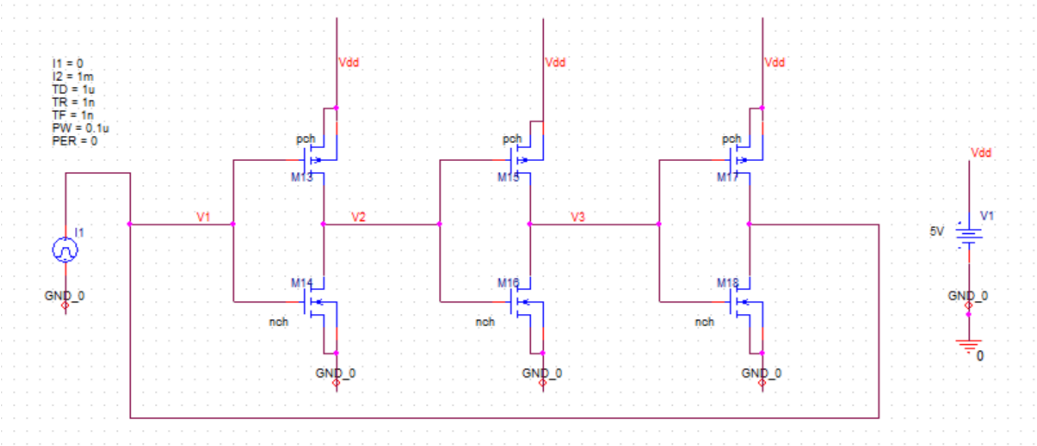
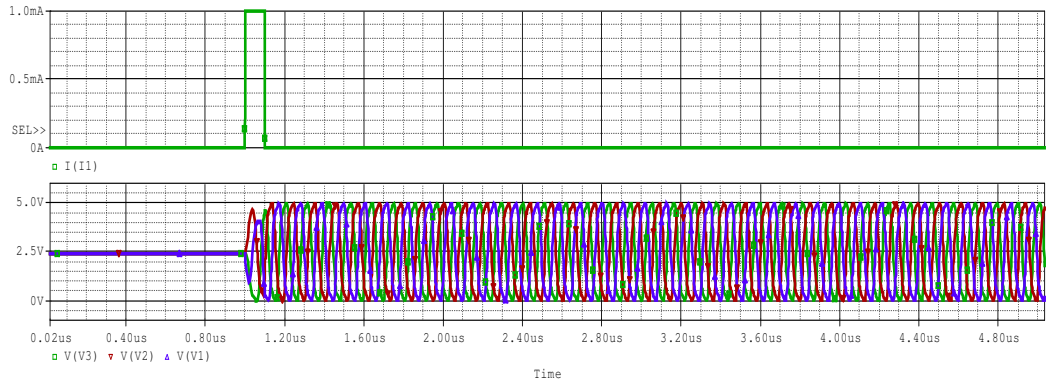
Parameter of Vpulse and Ipulse in Pspice



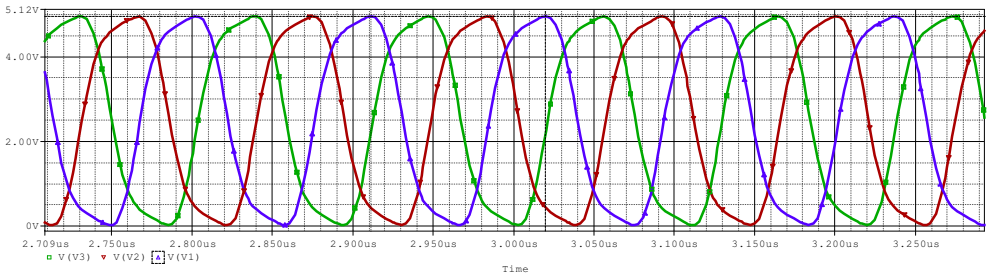
1. Ring Oscilator



Inject a short current pulse to node V1 at t=1us.



The oscillation starts when the Ipulse come. Here is the waveform after Ipulse has vanished.



First measure the delay of an inverter

Y1	Y2	Y1 - Y2
3.0384u	3.0198u	18.531n
4.5772	2.1801	2.3971
24.867m	438.158m	-413.291m
2.8045	4.9539	-2.1493

Read the time difference between 1 of V1 and next 0 of V2, so the response time:

$T_S = 18.5ns$

Then measure the period of the oscillator

Y1	Y2	Y1 - Y2
2.9113u	3.0198u	-108.540n
2.2204	2.1801	40.287m
427.579m	438.158m	-10.580m
4.9540	4.9539	130.075u

Read the time difference between two 1 in V1, so the period:

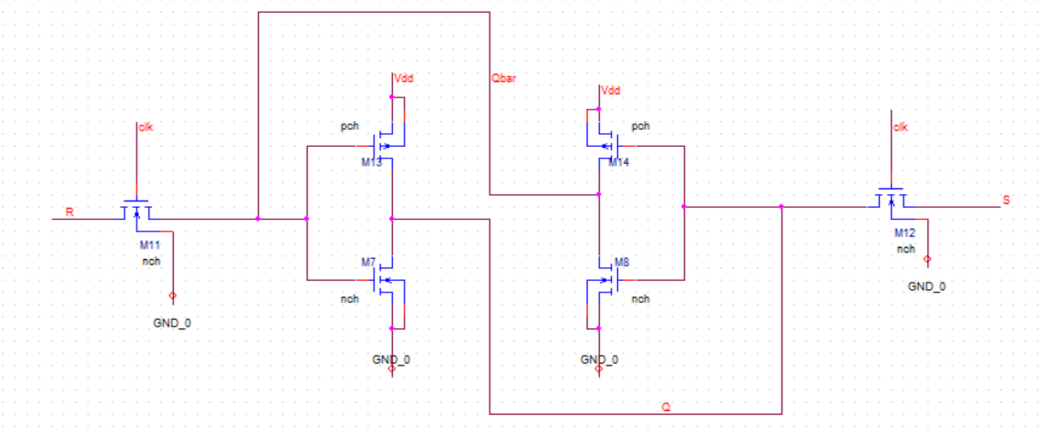
$\mathrm{T} = 108.5\mathrm{ns}$

So

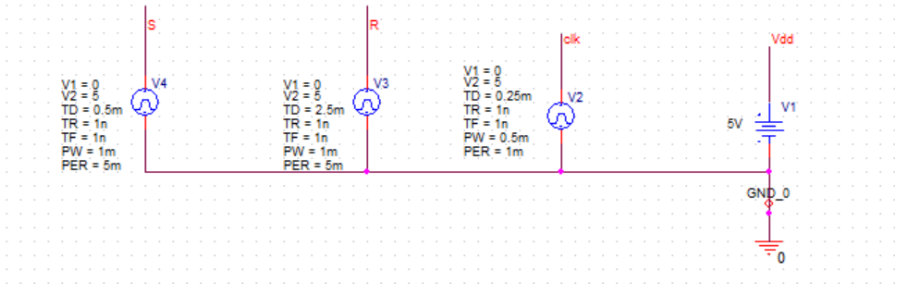
$\mathrm{T} \cong 5T_S$

2. SR Flip-Flop

I changed the definition of Q and Qbar to stay the same as textbook:



Input data, Clock and power supply:



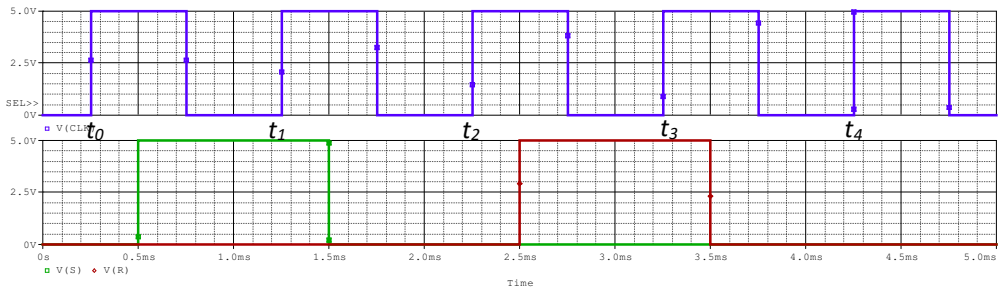
Run the simulation and plot all the input and output:

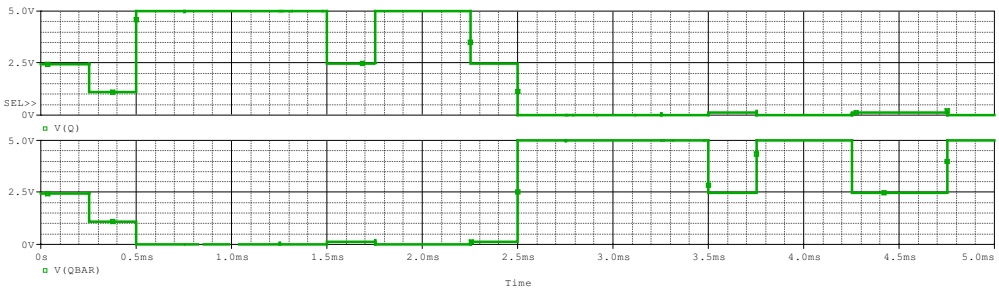
Figure 1 Clock

Figure 2 Set (Green) and Reset (Red)

Figure 3 Q

Figure 4 Qbar





Read the cases on the rising edge of the clock signal

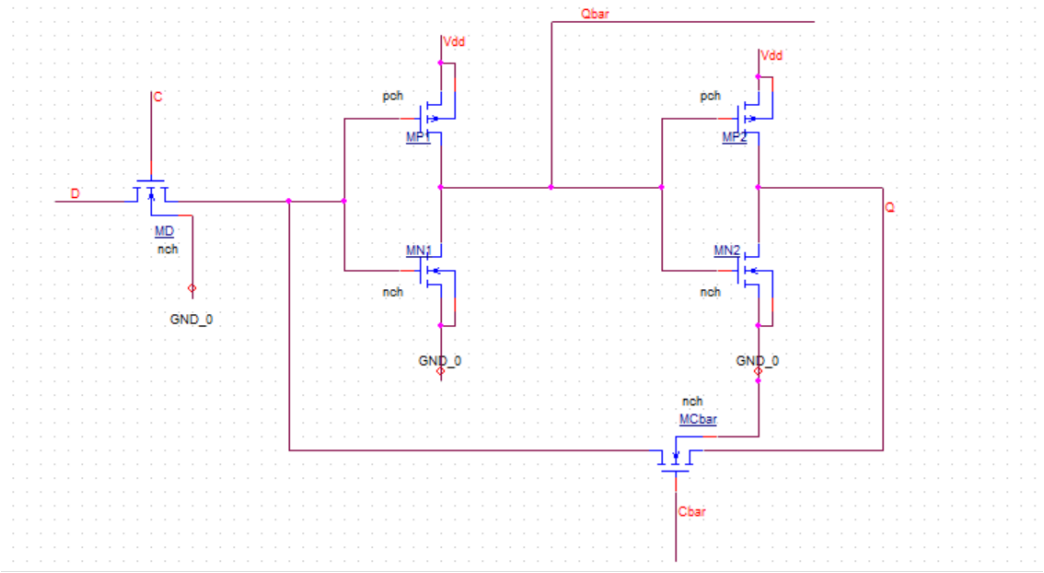
time	S	R	Q	Qbar	State
t0	0	0	N/A*	N/A	Latch
t1	1	0	1	0	Set
t2	0	0	1	0	Latch (=t1)
t3	0	1	0	1	Reset
t4	0	0	0	1	Latch(=t3)

*Initial state is not given so the flip-flop has no value to latch at t0.

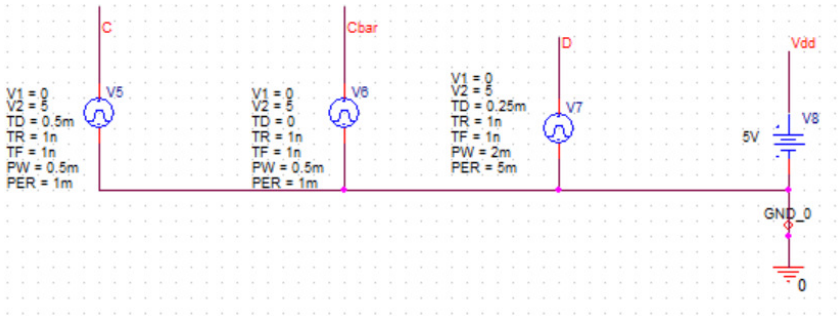
The voltage decrease in the latching stage, this comes from the non-ideal characteristic of the NMOS switch.

Reference: Pass Transistor Logic
https://en.wikipedia.org/wiki/Pass_transistor_logic

3. D Flip-flop



Input data, Clock and power supply:



Run the simulation and plot all the input and output:

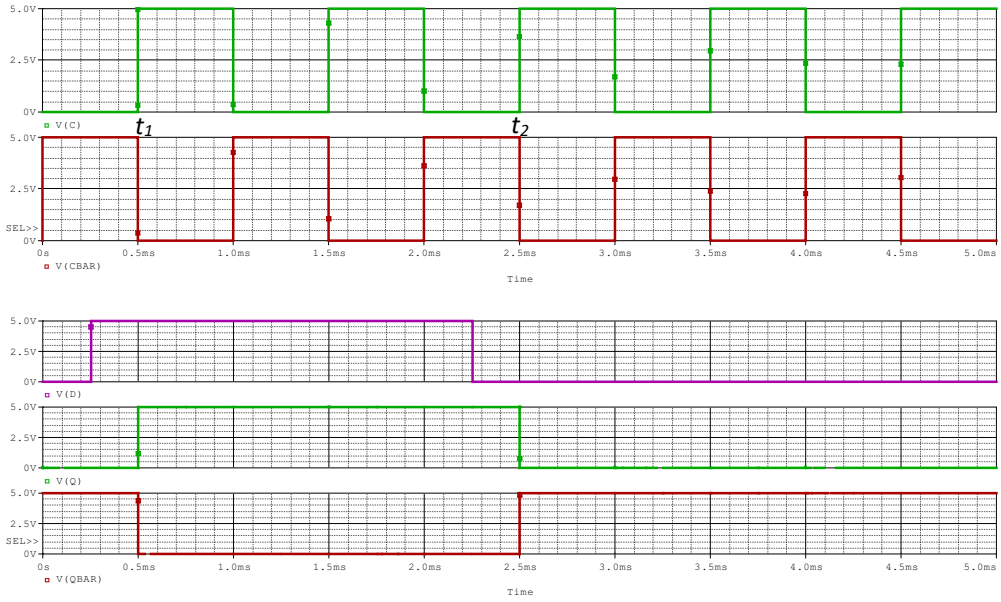
Figure 1 Clock

Figure 2 Clockbar

Figure 3 D

Figure 4 Q

Figure 5 Qbar



Read the cases on the rising edge of the clock signal

time	D	Q	Qbar
t1	1	1	0
t2	0	0	1

Q follows D at every rising edge of clock.

D flip-flop is edge triggered.

D becomes 1 before t1, but it’s not triggered until t1;

D becomes 0 before t2, but it’s not triggered until t2;