Solutions to Homework 5
Spring 2019
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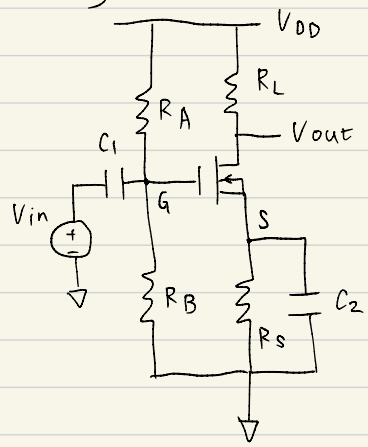
MOSFET Model:

```
.model nch nmos(Level=1 Tox=300n Uo=600 Kp=20.54u W=144u L=8u Vto= 1.3
+ Lambda=15m Cbd=4p Cbs=4p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)

.model pch pmos(Level=1 Tox=300n Uo=300 Kp=10.32u W=328u L=8u Vto=-1.5
+ Lambda=15m Cbd=8p Cbs=8p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)
```

Design

1a)



$V_{DD} = 6V$, $C_1 = C_2 = 10\mu F$, $R_S = 1k\Omega$

Use 4007 NMOS

$k_n' = 20.54u$, $V_{to} = 1.3V$

$W = 144u\,(m)$ $L = 8u\,(m)$, $\lambda = 15m\ (V^{-1})$

DC Bias Calculation

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_{to})^2 (1 + \lambda V_{DS})$$

$$\begin{cases} I_D = 0.5\,mA \\ V_{DS} = 3V \end{cases} \Rightarrow V_{GS} = 2.9088\,V$$

$$V_D = I_D R_S + V_{DS} = 0.5\,mA \times 1K\Omega + 3V = 3.5V$$

$$R_L = \frac{V_{DD} - V_D}{I_D} = \frac{6V - 3.5V}{0.5\,mA} = 5k\Omega$$

$$g_m = \frac{2 I_D}{V_{GS} - V_{to}} = \frac{2 \times 0.5\,mA}{(2.9 - 1.3)V} = 0.6216\,mS$$

$$g_o = \lambda I_D = 15 \times 10^{-3} \times 0.5 \times 10^{-3} = 7.5 \times 10^{-6}\,S$$

$$A_V = -g_m (R_L // r_o) = \frac{-g_m}{\frac{1}{R_L} + g_o} = -2.996$$

$$V_G = V_{GS} + I_D R_S = 2.909\,V + 0.5\,mA \times 1\,k\Omega$$

$$= 3.409\,V$$

$$\frac{R_A}{R_B} = \frac{V_{DD} - V_G}{V_G} = 0.76$$

$$R_A = 100\,M\Omega, \quad R_B = 131.58\,M\Omega$$

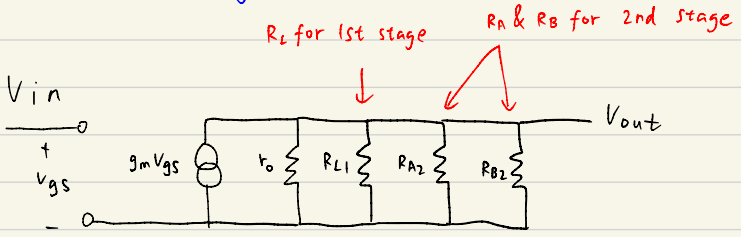
1C) $\frac{R_A}{R_B} = 0.76$, set $R_A = 10\,\Omega$

$\rightarrow R_B = 13.16\,\Omega$

for 2nd-stage

With the existence of 2nd stage amplifier, the small-signal equivalent circuit of 1st stage CS amplifier becomes:

[we treat bypass capasitor short at the frequency of the small signal here]

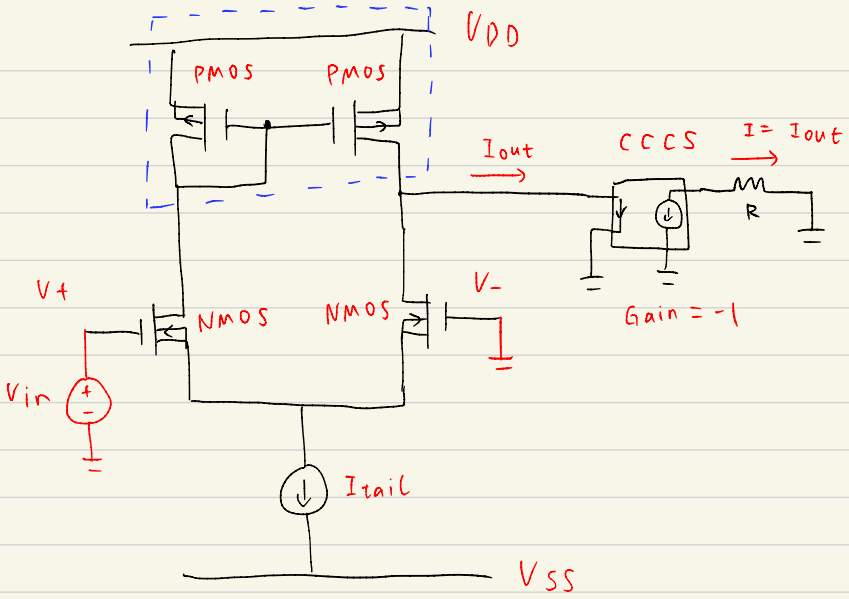


$$A_{V1} = \frac{V_{out}}{V_{in}} = -g_m (R_L // R_{L1} // R_{A2} // R_{B2})$$

when R_{A2} & R_{B2} big enough, they could be neglected in the A_{V1} expression, otherwise, A_{V1} will be much lower.

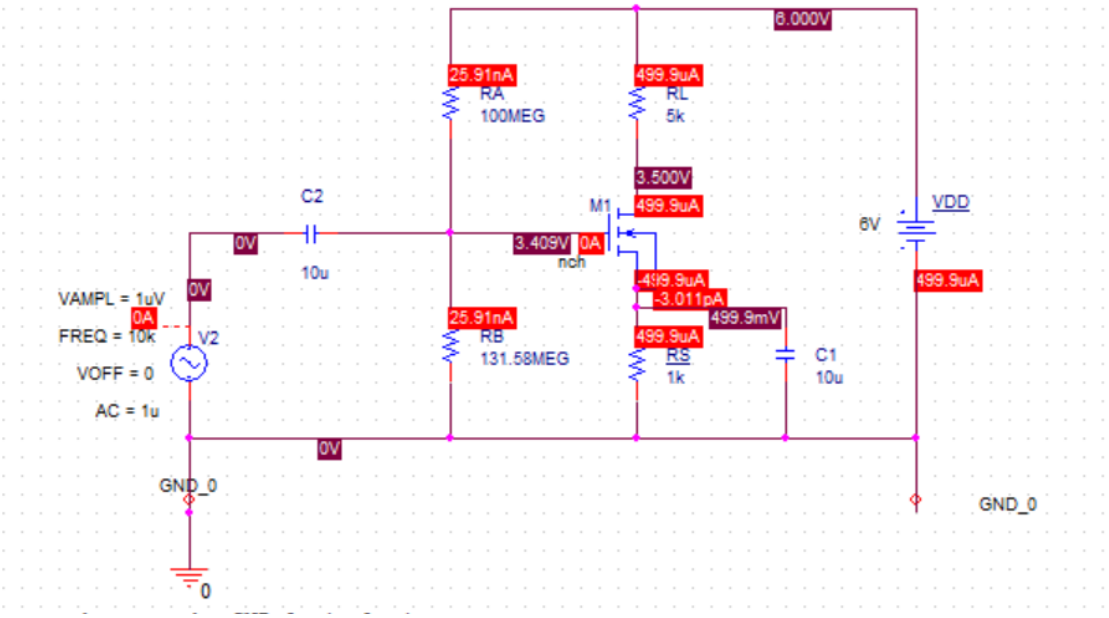
current sourcing mirror

2a)



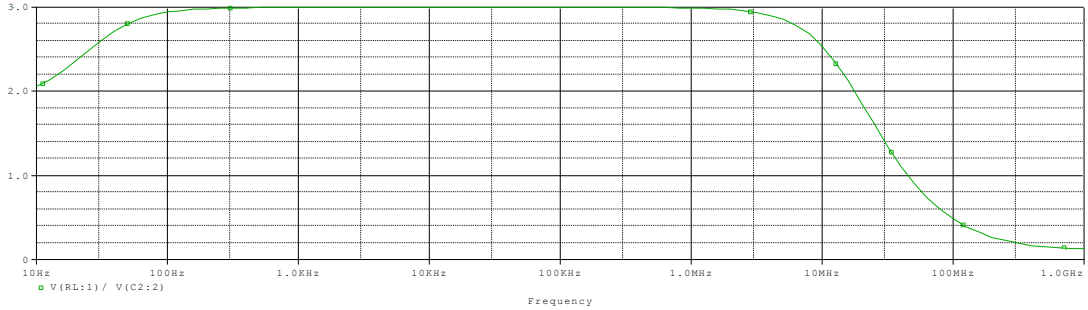
Check in Pspice:

1a)



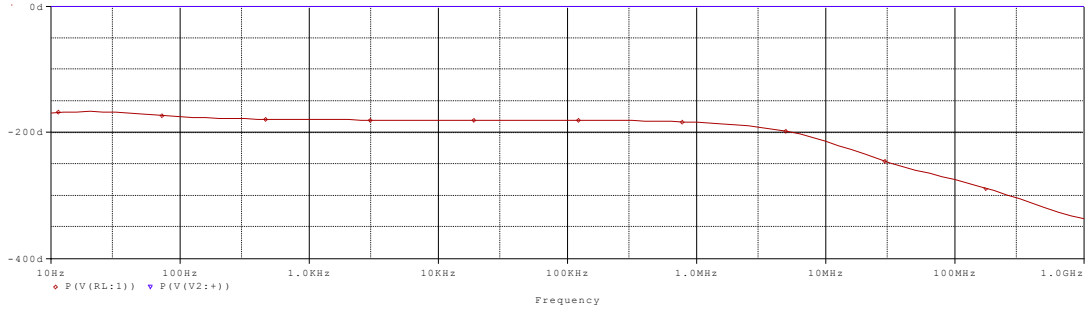
iD=500uA=0.5mA, and VDS=VD-VS=3.5V-0.4999V=3V

Use the method of frequency sweep to check the (mid frequency band) gain.



This plot shows the magnitude of Vout/Vin changes with frequency, so we can read from the curve that the magnitude of mid frequency band voltage gain is about 2.9981.

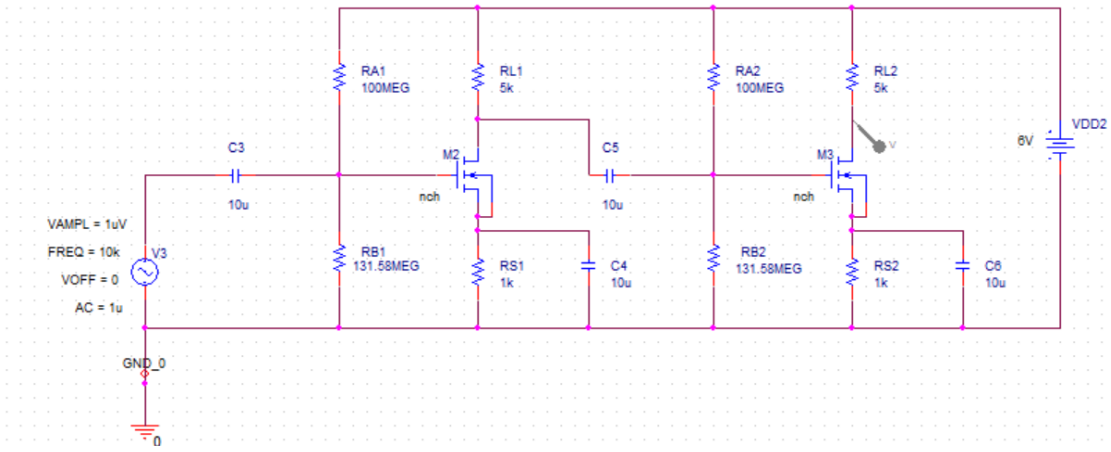
Trace Name	Y1
X Values	1.2711K
V(RL:1)/ V(C2:2)	2.9978



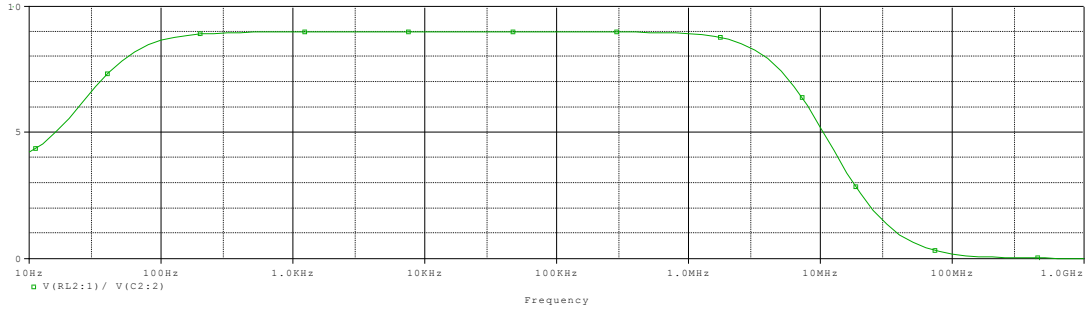
Phase response shows that the phase of voltage gain is about -180. So the voltage gain of the circuit is -2.9881.

1b)

Cascade two of the above circuits:

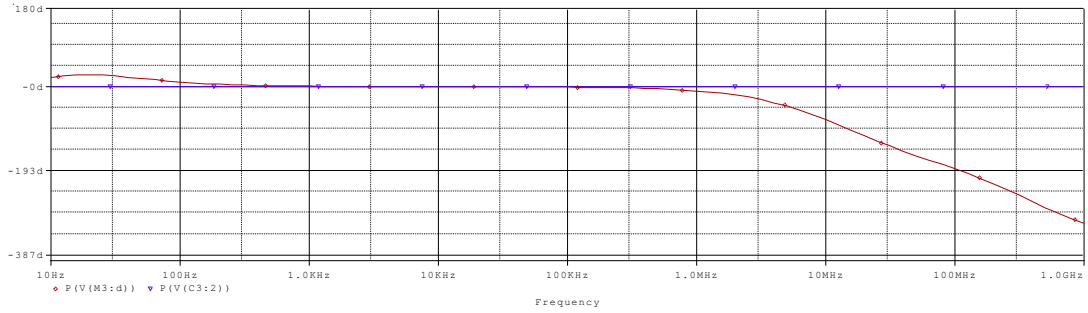


Magnitude of Vout/Vin frequency sweep:



Read from the plot that the magnitude of mid frequency band voltage gain is about 8.9879.

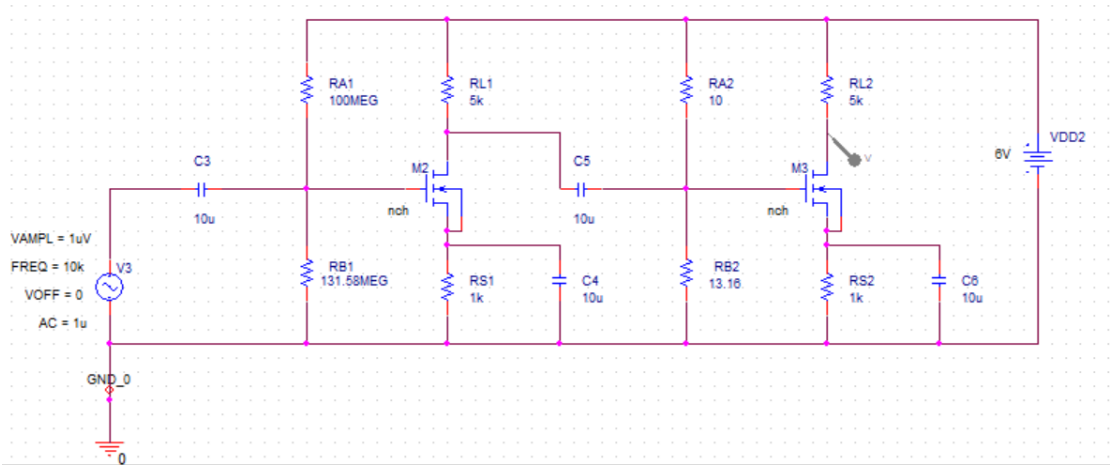
Trace Color	Trace Name	Y1
	X Values	5.2148K
CURSOR 1,2	V(RL2:1)/ V(C2:2)	8.9879



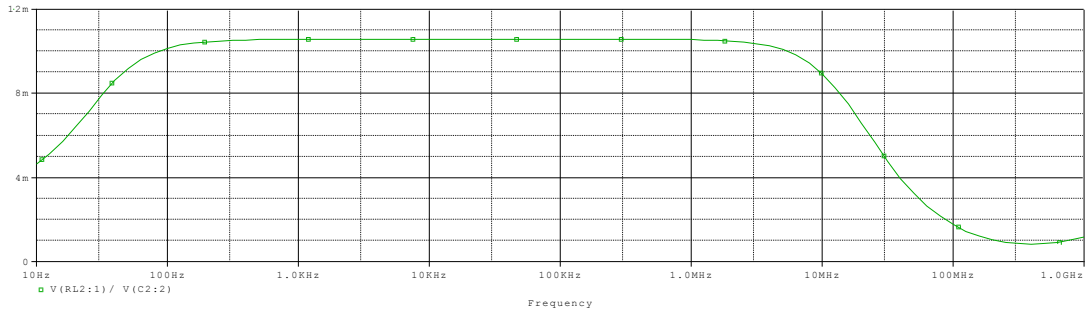
Phase response shows that the phase of voltage gain is about 0. So the voltage gain of the circuit is 8.9879, which is close to the square of one-stage voltage gain.

1c)

Change the second stage bias resistor:

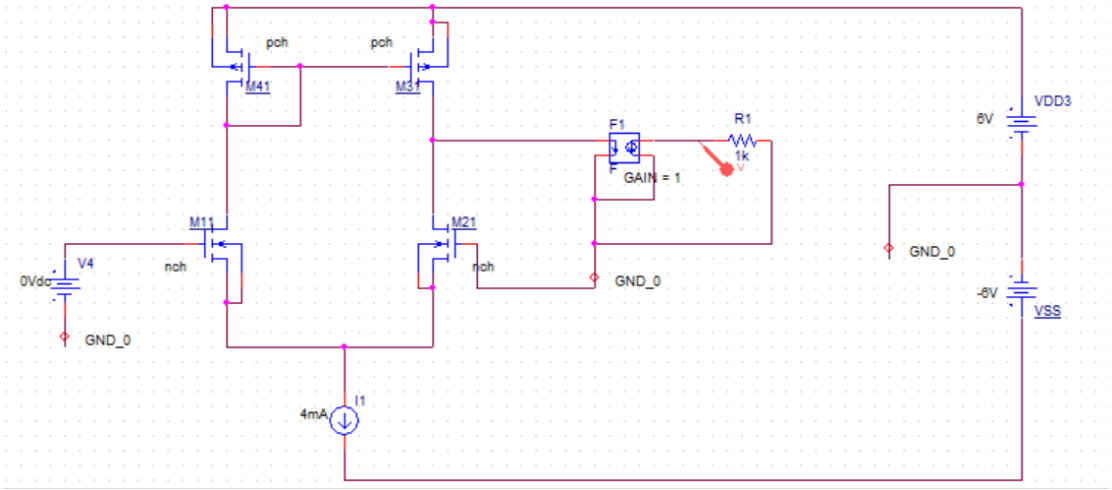


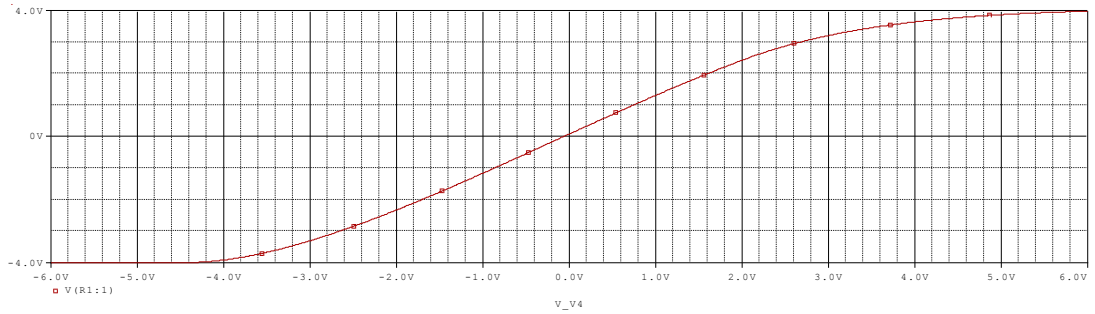
Frequency sweep:



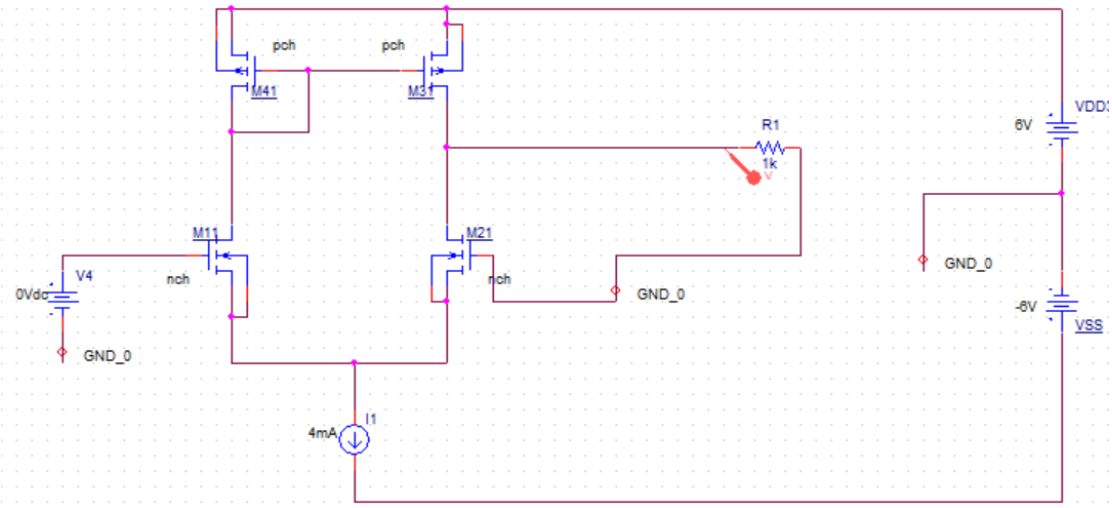
Mid frequency band voltage gain is around 5.70e-3, which is much lower than the result of 1b.

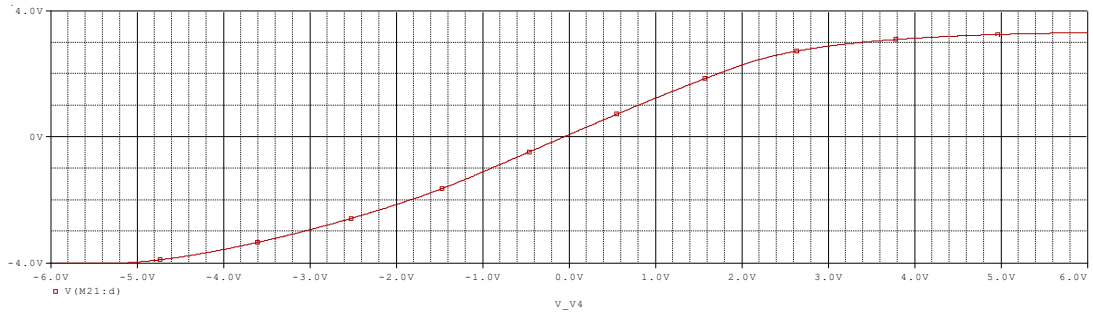
2b)





2c)





When connecting the load resistor to the OTA directly, output conductance is finite. So the output characteristic become less idea than the case where load resistor is isolated from the OTA circuit with CCCS (current controlled current source). We can see from the plot that output current can't reach tail current when Vin is close to VDD.