Solutions to Homework 2

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1a (20 Points)

Model of the PMOS and NMOS in CA3600E.

.model nch nmos(Level=1 Tox=300n Uo=600 Kp=20.54u W=144u L=8u Vto= 1.3

+ Lambda=15m Cbd=4p Cbs=4p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)

.model pch pmos(Level=1 Tox=300n Uo=300 Kp=10.32u W=328u L=8u Vto=-1.5

+ Lambda=15m Cbd=8p Cbs=8p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)

In simulation, use the breakout model of MOSFET in BREAKOUT library, which names Mbreakn and MBreakp, and copy the parameters to edit PSpice model.



For PMOS and NMOS working in saturation mode:

Current flowing through PMOS:

 

Where

 

Current flowing through NMOS:



Where

 

Since PMOS and NMOS are connected in series, the current flowing through these two MOSs should be the same.

 

From (1) to (5), we have:

(6)

Using the parameter of model CA3600E,

Kpn=20.54uA/V2, Wn=144um, Ln=8um, λ=15e-3, VTO-n=1.3V，

Kpp=10.32uA/V2, Wp=328um, Lp=8um, λ=15e-3, VTO-p=-1.3V，

For VDD=5V and VSS=-5V, both PMOS and NMOS are working in saturation mode

Solve equations (6) in matlab,

Vout = 20.85mV

Run the simulation in BIAS point.



|  |
| --- |
| VDD=5V and VSS=-5V |
| Hand calculation  | Simulation |
| 20.85mV | 20.76mV |

The results are very close.

For VDD=3V and VSS=-3V, both PMOS and NMOS are working in saturation mode

Solve equations (6) in matlab,

Vout = -45.53mV

Run the simulation in BIAS point.



|  |
| --- |
| VDD=3V and VSS=-3V |
| Hand calculation  | Simulation |
| -45.53mV | -45.55mV |

for VDD=1V and VSS=-1V,

Notice that the absolute values of these two voltage source are less than the turn-on voltage. As a result, both MOSs are working in cut-off mode. So you cannot use (1) to (5) to solve these problem. You don’t need to do hand calculation for this particular problem, simulation is enough.

Run the simulation in BIAS point.



|  |
| --- |
| VDD=1V and VSS=-1V |
| Hand calculation  | Simulation |
|  | -56.06e-18V |

b. (20 points)



Both two transistors are working as a diode. You can do simulation only.

|  |  |
| --- | --- |
|  | Vout |
| VCC=5V and VEE=-5V | 1.122V |
| VCC=3V and VEE=-3V | 782.2mV |
| VCC=1V and VEE=-1V | 305.1mV |

c. (20 points)

Choose a pair of models in Bicmos12 and change the W and L of the models.

Set the width of PMOS as a parameter and sweep the parameter.

bicmos12.lib needs to be loaded in the library portion of the configuration files under edit simulation profile menu. Path: c:\cadence\SPB\_17.2\tools\pspice\library\bicmos12.lib



Run simulation in Pspice using above circuit,  such that output voltage is zero.



2.

a. (20 points)



Run in DC sweep with Vin from -5V to 5V:



Find the points where the curve intersects with X-axis and Y-axis.



Vin=0: (Run in the BIAS point)



Vout=0: (close to zero)



|  |  |
| --- | --- |
| Vin = 0V | Vout = 848.6mV |
| Vin = 21mV | Vout = 0V |

In problem 1, the MOSs will always work in saturation mode as long as the voltage of battery source is large enough. But for problem 2, Vin should be selected within a narrow range such that both MOSs are working in saturation mode.

For NMOS, to work in saturation mode, inequality (11) should be satisfied,

  (11)

For this problem, (11) is equivalent to (12)

 (12)

For PMOS, to work in saturation mode, inequality (13) should be satisfied,

 (13)

For this problem, (13) is equivalent to (14),

 (14)

Solve (12) and (14) in Pspice, the area where yellow and pink curve below zero, red and blue curve above zero is the solution.





The range is quite narrow, which was about -17mV-53mV.

b. (10 points)

Set Vin = 21.2mV, Vac = 0.1 (or other small values)





c. (10 points)



Secondary sweep is used:



As Vdd increases, the Vin that corresponds to Vout =0 increases.

Vdd=2-5V, the MOSs are working above threshold. When input voltage is 0V, output voltage will increase as Vdd increases.

But for Vdd = 1V, the MOSs are working in cut-off mode.