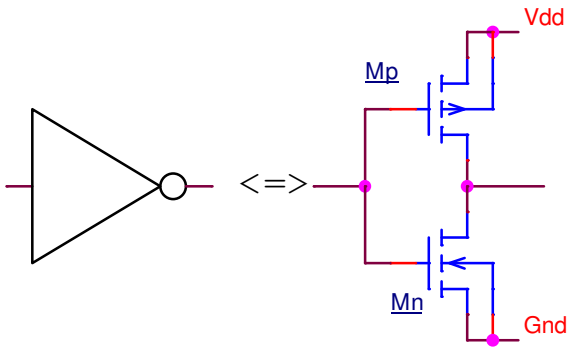
File: H:/coursesS19/303/303S19Hmwk6.doc RWN 04/22/19

ENEE 303Spring 2019 – Homework 6 Due Th 05/02/19

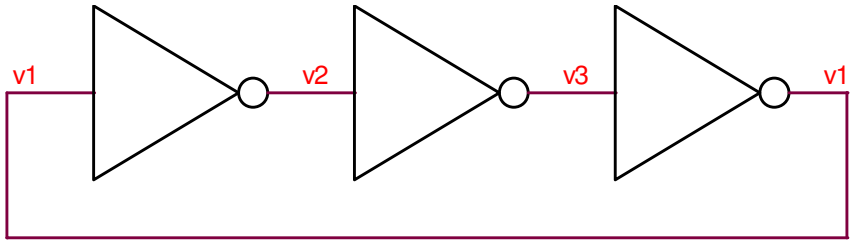
For the following use 4007 CMOS transistors for the inverters. And use Vpulse for clocks and data (amplitudes of ground=digital 0 and Vdd=5V=digital 1 and in the milliSec range). In the following Cbar and Qbar represent digital complements of the clocks C and outputs Q.

The inverters are symbolized by:



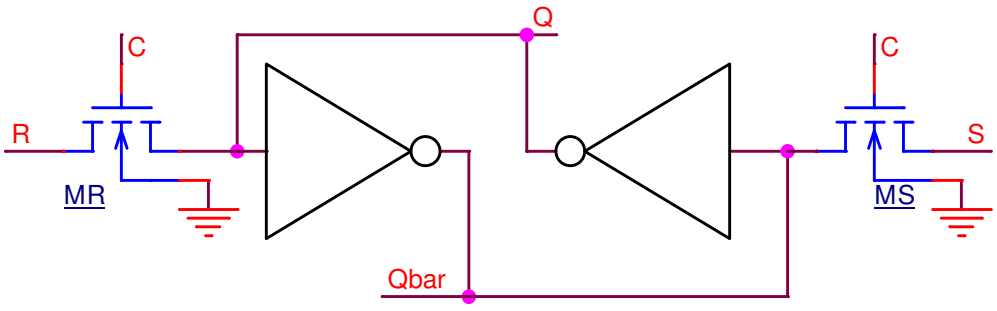
For all of the following run Spice to investigate desired behavior. Submit your Spice runs.

1. (30 points; 3 stage inverter ring oscillator; Figure 16.28 of Sedra/Smith, p. 1275)



In order to begin oscillations you might place a short current pulse into the v1 node.

2. (35 points; Clocked (set-reset) SR flip-flop: Figure 16.7 of Sedra/Smith, p. 1247)



3. (35 points; (Data), D flip-flop: Figure 16.9 of Sedra/Smith, p. 1248)