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ENEE 303Spring 2019 – Homework 5 New due date Th 03/14/19

1. (60 points; Cascade CS design) [revised]
   a) Using an NMOS 4007 transistor. Design a common source amplifier for a small signal voltage gain when biased at the Q point ID=0.5mA, VDS=3V [note that this determines VGS]. Calculate the voltage gain. For this use a 6 Volt battery (for VDD choosing VSS=0). Use coupling and bypass capacitors of 10 uFarad (u=micro=10^{-6}), a source resistor of 1 KOhm (K=kilo=10^{3}) and gate biasing resistors so that the smallest one is 100 MegOhms (Meg=10^{6}) or larger. Check by using Spice that the (mid frequency band) gain is close to -8. Explain why your means of checking this gain is valid.
   b) Cascade two of the above circuits and check in Spice that the small signal voltage gain is close to 64.
   c) Change the gate bias resistors on the second stage (but not on the first stage) so that the smallest is 10 Ohms. Check the two-stage mid band gain and discuss the change over the result of part b.

2. (40 points, CMOS OTA)
   a) Design an OTA using CMOS transistors. Choose a tail current of 4 mAmp (m=milli=10^{-3}), use two= batteries for VDD=6V=-VSS, and feed a Spice F component (=CCCS) with its other input connected to ground and its outputs across a 1KOHM resistor (also one terminal connected to ground.
   b) Do a DC run on the input voltage where the negative OTA input terminal is grounded. Sweep the input voltage from VSS to VDD and record the voltage on the load resistor.
   c) Replace the CCCS by the 1 KOhm load resistor (that is, place it directly at the OTA output with its other terminal to ground) and check the voltage on the resistor. Compare DC sweep results with the result of a).