File: G:/coursesS19/303/303S19Hmwk3.doc RWN 02/14/19

303 Spring 2019 – Homework 3 due Th 02/21/19

The transistors are ones used in teaching labs here; some useful data is on the course web page. For the MC4007=CA3600 CMOS models use KP, W, L, Vto and Lambda. Curves are on the web page and KP is k in the text book.

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.model nch nmos(Level=1 Tox=300n Uo=600 Kp=20.54u W=144u L=8u Vto= 1.3
+               Lambda=15m Cbd=4p Cbs=4p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)
.model pch pmos(Level=1 Tox=300n Uo=300 Kp=10.32u W=328u L=8u Vto=-1.5
+               Lambda=15m Cbd=8p Cbs=8p Cgdo=1.7n Cgso=1.7n Rs=1 Rd=1)
```

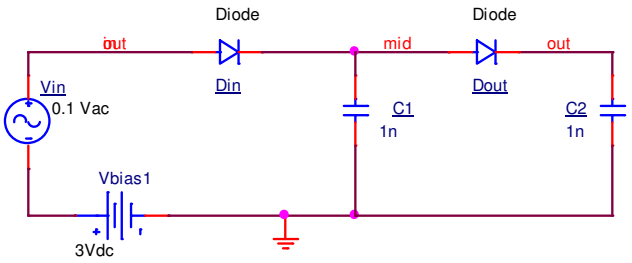
1. (35 points, Q point values)
   a. For the NMOS transistor assume a Q point in the saturation region at VDS=VGS= 7V. Find the bias current ID.
   b. Repeat for the Q point in the triode region at VDS=2V and VGS=5V.
   c. Repeat for the PMOS transistor with a Q point at VDS=VGS=-7 and cpmpare with the result of part a.

2. (35 points, CMOS Y matrix)
   a. For the NMOS of Problem 1 above biased at the two stated Q points give the low frequency small signal admittance matrices (one for each Q point)
   b. Repeat for the PMOS in saturation.
   c. Draw the small signal equivalent circuits for each transistor when in saturation and compare. Be sure to label g, d, and s nodes.

3. (30 points, CS amplifier)
   Assume a common source NMOS 4007 transistor is biased at the Q point of Problem 1 above with a 9V power supply (=VDD).
   a) Find the load line resistor resistance R_L and sketch the load line on a copy of the NMOS transistor curve.
   b) Give the ideal voltage gain $A_v = -g_m R_L$ and compare with the voltage gain in the presence of the transistor output resistance r_o.
   c) Give gate bias resistors in the MegOhm range to achieve the Q point and Av.

3. (50 points, CMOS biasing)
Separately bias the two amplifiers of problem 2 and check in Spice your circuits' time domain responses to an input 2KHz sinusoid of 5mV amplitude.

Older holdover:
From possible homework 1:
2. (50 points, Diode biasing and ac & transient analysis).
For the following voltage multiplier circuit assume that the diodes are 1N4007s working at room temperature.
a) For this circuit calculate by hand the bias point (= Q point) current and voltage of the diode.
b) Determine (also by hand) the small signal gain of the circuit vo(s)/vi(s), first with symbols (r_d, R_1, L, R_L) and then with numerical values.
c) Set up the circuit in Spice and: b1) check the simulated Q point, then b2) do a magnitude frequency response (=AC run) from 1Hz to 1MEG Hz.
d) Comment upon your simulation results versus your hand calculation.

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