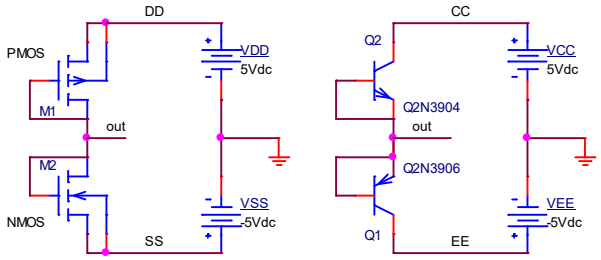
File: G:/coursesS19/303/303S19Hmwk2.doc RWN 02/07/19

303 Spring 2019 – Homework 2 due ~~Th 02/14/19~~ ==> Tu 02/19/19

1. (60 points, transistor voltage dividers)



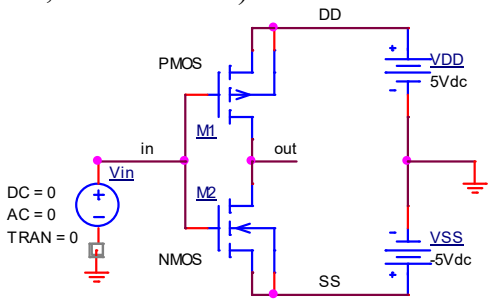
a) For the CMOS circuit on the left above calculate the output voltage using the saturation equations with model data for 4007 CMOS transistors (use their KPs, VTOs and LAMBDAs from their CA3600 models). Check your calculation in Spice [possible via breakout transistors with CA3600 models] (you can use BIAS data [preferable] or a dc run on one of the batteries through the given VDD). Change the battery voltages to ±3V and again to ±1V and repeat.

b) Repeat for the BJT circuit shown using the Q2n3904 and Q2n3906 transistors.

c) Replace the CMOS transistor by 0.5u models (use BICMOS12 library ones) and adjust the PMOS width in Spice (convenient via PARAM runs) so that the voltage at the output node (with respect to ground) is 0 (when the batteries are at ±5V).

d) Submit relevant circuits, new model parameters, and curves; comment upon the results.

2. (40 points, MOS inverter)



a) For this inverter circuit using 4007 transistors do a Spice DC run varying the input voltage from VSS (=-5V) to VDD (=+5V) in small steps and plot the out(put) node voltage versus the in(put) voltage. Give the value of V(out) when V(in)=0 and comment upon the relationship to problem 1 above; also give the value of V(in) to make V(out)=0. Also note over which values of Vin the transistors are in saturation (that is check when VDS>VGS-VTO which can be done with PSpice curves).

b) Do an AC run from 1Hz to 100MegHz with the DC offset of Vin set to give V(out)=0 when V(in =0).

c) Make VSS=-VDD by using a (global) parameter and repeat a) with a parametric run for 1≤ VDD ≤5 stepped in 1Volt steps. Comment on the results.