ENEE 307: Electronics Analysis and Design Laboratory: Part I

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Laboratory 1

Diodes and Operational Amplifiers

1.1   introduction

In this lab you will build and learn about diode circuits, power supplies, op-amp comparators and amplifiers. To maximize your learning, you must know what you are doing before coming to lab. This means reading the lab and answering the preliminary questions at the end of this chapter. You must hand in answers to the questions before you start doing the lab. Have fun.

1.2   Diodes and Rectifier Circuits

Diodes are semiconductor devices that allow current to flow in only one direction.[1] Diodes are composed of a junction between a P-type semiconductor and an N-type semiconductor. Most diodes are made of silicon. Silicon diodes turn-on strongly when the p-side is made approximately 0.7V higher than the n-side. The expression relating current through a diode to the voltage applied across a diode is given by:

$$I_d = I_S \left(exp\frac{V_d}{V_t} - 1 \right) \tag{1.1}$$

where I_d is the diode current. V_d is the voltage from the p-side to the n-side. V_t is called the thermal voltage which comes from basic physics and is equal to $0.026V$ at room temperature. I_S is the saturation current which depends on the way the diode is fabricated. I_S can be obtained from data books from specific diode manufacturers. From equation (1.1), it is clear that when $V_d \gg V_t$, a large current can flow. However, when $V_d < 0$ a negligibly small reverse saturation current will flow.

Diodes have many electronic applications. In this lab we will demonstrate that the diode is a rectifier, and then show how a rectifier can be used with a transformer to construct a

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[1]Strictly speaking a diode has a very small reverse current, but this is so small that we almost always neglect it.

DC power supply from AC wall current. You will then use the power supply you make to power op-amp circuits.

1.2.1   Experiment: Simple Half-Wave Rectifier:

1. Set up the circuit in Fig. 1.1. For this circuit and all others in this lab, use the 1N4007 diodes that are in your lab kit.
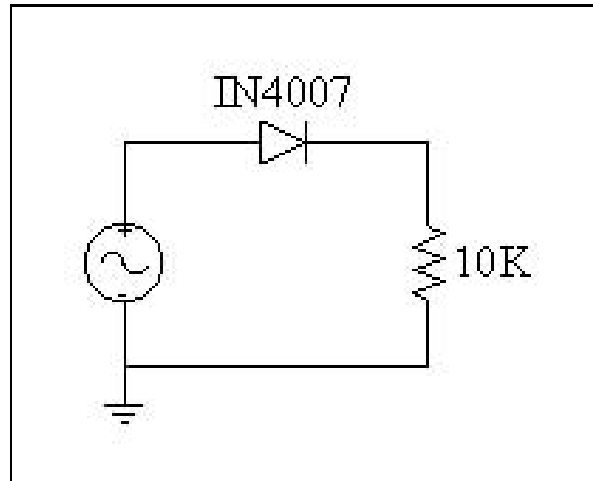
Figure 1.1: Positive Half-Wave Rectifier

   Set the signal generator to 1kHz with and amplitude of approximately 5V. (Make sure the DC offset on your signal generator is zero.) Sketch the input versus the output as a function of time. Note the difference in voltage between the input and output You should see that only current flowing in the positive direction with respect to the voltage of the signal generator. That is, during the positive half of the cycle, the diode is forward biased, thereby letting current through. During the negative half, the diode is reverse biased and no current can pass.

2. Reverse the polarity of the diode (turn it around). Now repeat the above exercise. What's the difference in output versus input signals with the diode reversed.

3. Increase the frequency of your signal generator from 1kHz to 10kHz, 100kHz and 1MHz. What happens, can you think of a reason why?

4. Set the signal generator back to 1kHz. Calculate the average power being dissipated in the resistor. Recall that average power is given by:

$$P_{avg} = \frac{1}{T} \int_0^T v(t)i(t)dt \qquad (1.2)$$

   Where T is one period of the signal.

1.2.2 Experiment: The Full Wave Rectifier

We observed that in the half-wave rectifier, we lost half of our signal. To take advantage of the entire signal we use the full-wave rectifier which is shown in Fig. 1.2.
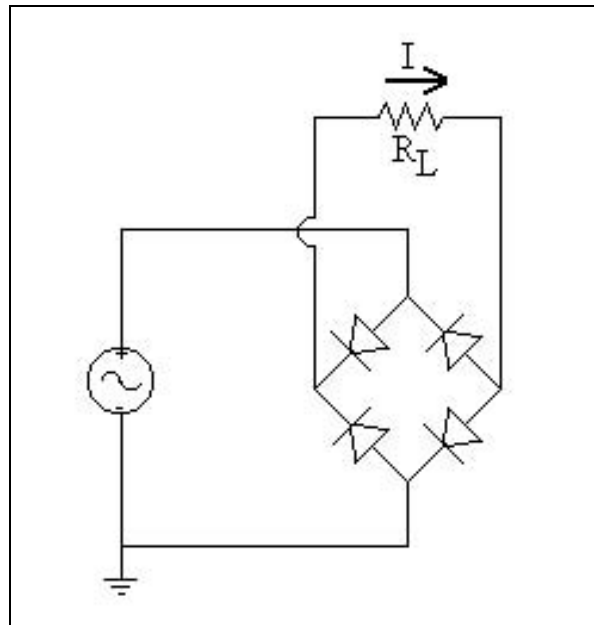
Figure 1.2: Full-Wave Rectifier

If you follow the current path through a full wave rectifier you will notice that when V_{in} goes positive, D_2 and D_4 are on (conducting), while D_1 and D_3 are off, and current flows in the direction through the resistor as indicated by the arrow. When V_{in} goes negative, D_1 and D_3 are on (conducting), while D_2 and D_4 are off, and current flows in the same direction through the resistor as indicated by the arrow. So, during both halves of the cycle current flows through the load resistor in the same direction, and the entire signal is used.

1. Set up the circuit in Fig. 1.2, with $R_L = 10K$. Set the signal generator to 1kHz with and amplitude of approximately 5V. (Make sure the DC offset on your signal generator is zero.) Sketch the input versus the output as a function of time. Remember, the output is the voltage across the 10K resistor. You may find it easiest to measure the drop across the 10K resistor with two probes.

2. Calculate the average power dissipated in the resistor. Compare this value to that of the half wave rectifier. Which circuit can provide more power to a load?

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1.3 DC Power Supplies

1.3.1 Half-Wave Single-Sided Supply

A typical application for diodes is in the conversion of an AC signal into a constant DC signal which can then be used to power electrical circuits. To make such a circuit we'll use the 24V transformers provided. These transformers take the wall signal of approx 120Vrms and drop it down to 24Vrms at a frequency of 60Hz. By attaching a rectifier we can transform the AC signal so that it only passes load current in one direction. Finally, if we filter the signal out of the rectifier, we can obtain a fairly constant DC signal that can be used as a power source for electronic circuits. Power circuits similar to these are found in virtually all electronic equipment, including computers, stereos and televisions.

To understand how the filter works, consider the circuit shown in Fig. 1.3. As the signal
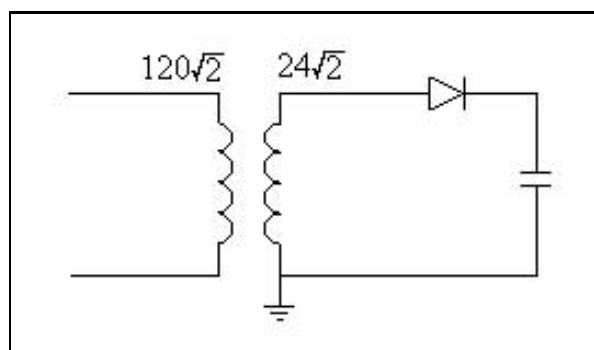
Figure 1.3: DC Power Supply without Load

at V_o increases, the capacitor charges up virtually instantaneously since there is very little resistance in the circuit. After the waveform reaches its peak value and starts to decrease, the voltage on the capacitor is higher that the voltage going into the rectifier. Thus, the diodes will be reverse biased, and no current will flow out of capacitor so it cannot discharge. Thus, the capacitor will be pinned at the peak voltage of the AC signal. Now, if we attach a load resistor R_L across the capacitor, as shown in Fig. 1.4, the capacitor will discharge through R_L with time constant $\tau = R_L C$.

If we make C very large so that $R_L C$ is much larger than the period of the AC signal we're rectifying, then the capacitor will not have very much time to discharge, and the output voltage will be almost constant with only a small AC ripple. To approximately determine the amount of AC ripple, we can start from the definition of capacitance

$$V = \frac{Q}{C} \tag{1.3}$$

Differentiating both sides with respect to time gives

$$\frac{dV}{dt} = \frac{1}{C}\frac{dQ}{dt} = \frac{I}{C} \tag{1.4}$$

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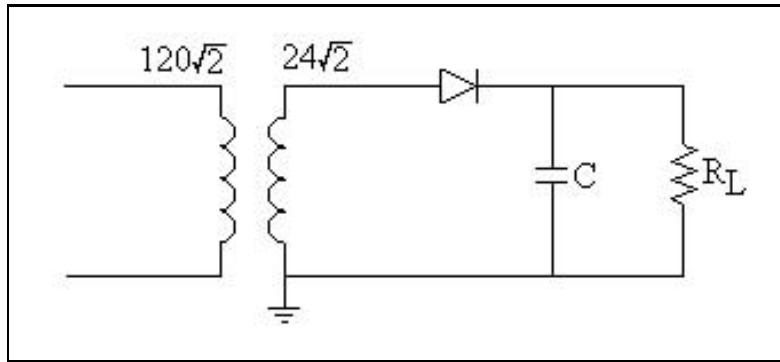
Figure 1.4: DC Power Supply with Load R_L

Multiplying out by the small time interval Δt yields to first order:

$$\Delta V = \frac{I}{C}\Delta t \tag{1.5}$$

If we take Δt to be approximately the period of a cycle of signal we are rectifying, then $\Delta t \approx \frac{1}{f}$, and the ripple voltage is proportional to the current through the load and inversely proportional to the frequency of the source voltage

$$\Delta V = \frac{I}{fC} = AC \; ripple \tag{1.6}$$

Finally, if the current is used to drive a load R_L, then the ripple voltage can be approximated by

$$\Delta V = \frac{V_{avg}}{R_L fC} = AC \; ripple \tag{1.7}$$

where V_{avg} is the time average voltage delivered to the load. Clearly, from a practical point of view, the more current that is required by the load, the greater the ripple and the less constant the DC voltage and the less ideal the DC power supply.

1.3.2   The Full-Wave Single-Sided Power Supply

We observed that in the half-wave rectifier, we lost half of our signal. To take advantage of the entire signal we construct a power supply with the full-wave rectifier which is shown in Fig. 1.5.

   To transform this signal into an almost constant DC value, we filter it using the same procedure as for the half wave rectifier and power supply. Only this time the ripple voltage should be approximately half of what it was before, since the capacitor will discharge for half the time as it did for the half-wave case. Thus, the AC ripple will be given by

$$\Delta V = \frac{V_{avg}}{2R_L fC} = AC \; ripple \tag{1.8}$$

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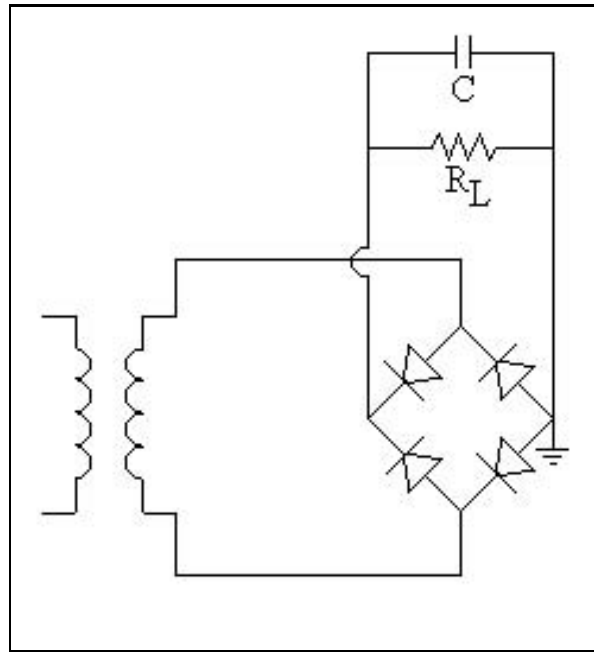
Figure 1.5: Full-Wave Supply with Step-Down Transformer

1.3.3 Experiment: The Full Wave Rectifier and Power Supply

1. Obtain a transformer from the instructor. The low side of the transformer has three wires coming out of it. The wires with the little pieces of tape are connected to the ends of the coil. The other wire is a center tap. For this experiment, let the center tap float while being careful not to short it to anything that will draw current. Plug in your transformer and measure the voltage across it using the scope. Sketch the waveform.

2. First, set up the circuit in Fig. 1.5, with $R_L = 10K$, except without the capacitor. After setting up the circuit, sketch the output as a function of time.

3. Now, place the $2200\mu F$ capacitor across the output as was done above. Now, measure the AC ripple for the three load resistors $R_L = 5K$, $10K$, $100K$. Calculate what the ripple should be for the capacitors and compare the calculated and measured values. (BE CAREFUL, THE ELECTROLYTIC CAPACITORS ARE POLAR, MAKE SURE YOU PUT THE NEGATIVE SIDE TO THE LOWER VOLTAGE, OTHERWISE.....)

1.3.4 Experiment: Design of Dual Output Power Supply

1. Using the circuit in Fig. 1.6 as a guide, build a dual sided power supply. A capacitor value of $2200\mu F$ will be used to design and construct a power supply with positive and negative $\pm 17V$ supply rails. (Rail means maximum (+) or minimum (-) power supply

voltage.) What AC ripple do you expect this supply to have if it drives a 10K load on either side.

2. Be careful putting your supply together because you will use it for the next part of the lab.
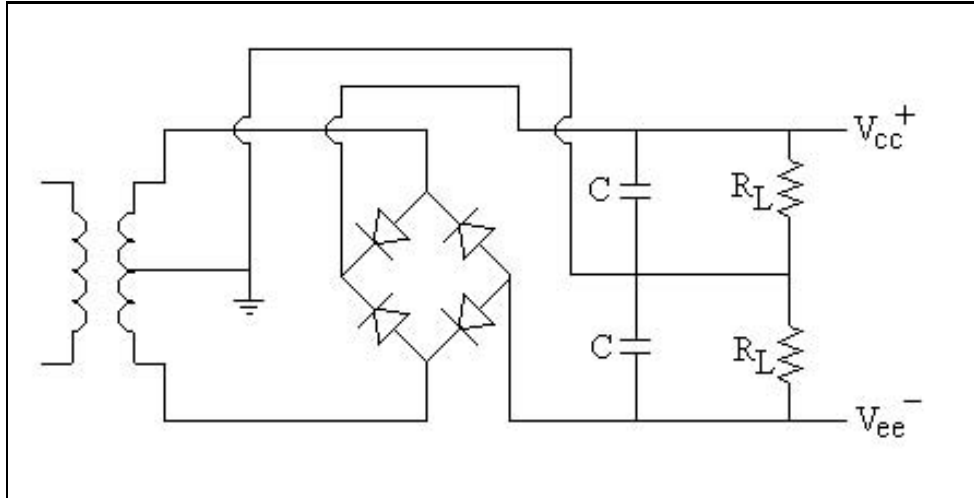
Figure 1.6: Dual Output Power Supply Circuit

1.4 Operational-Amplifier Review

This part of your lab is to provide a review of op-amps, and to give you an opportunity to use the power supply circuit you made in a real application. Recall that an op-amp is a three-terminal integrated circuit. Inside the op-amp is a fairly complicated circuit which typically consists of more than thirty transistors. Later in this course you will be constructing your own op-amps out of transistors. However, for now we will treat the op-amp as a black-box with the following equivalent circuit:

Fig. 1.7 shows that the op-amp can be described as a voltage controlled voltage source where the output voltage is proportional to the voltage across the input resistance R_{in}. Recall that most op-amps have extremely high input resistance, low output resistance, and extremely high gain. For example, the ubiquitous 741 op-amp has $R_{in} = 2M\Omega$, $R_{out} = 40\Omega$, and gain $A_v = 200,000$. For most applications, it's appropriate to treat an op-amp as ideal. For an ideal op-amp $R_{in} = \infty$, $R_{out} = 0$, and $A_v = \infty$. Under the ideal approximation, using an op-amp in circuit design is extremely simple.

An ideal op-amp without feedback is simply a comparator, where the output switches to the positive rail if $V^+ > V^-$, and switches to the negative rail if $V^+ < V^-$.

Once feedback is connected, the infinite gain forces $V^+ = V^-$. As a result, we can find the closed loop voltage gain very easily.

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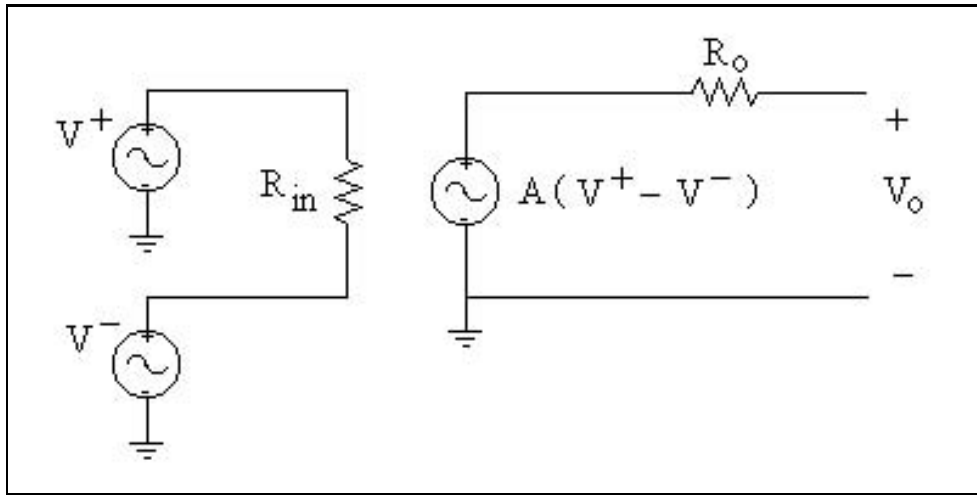
Figure 1.7: Operational Amplifier Equivalent Circuit

1.4.1 Noninverting Amplifier

Voltage Gain

The circuit in Fig 1.8 is the noninverting amplifier configuration, which has the signal V_{in} to be amplified going into V^+ and the feedback going to V^-.
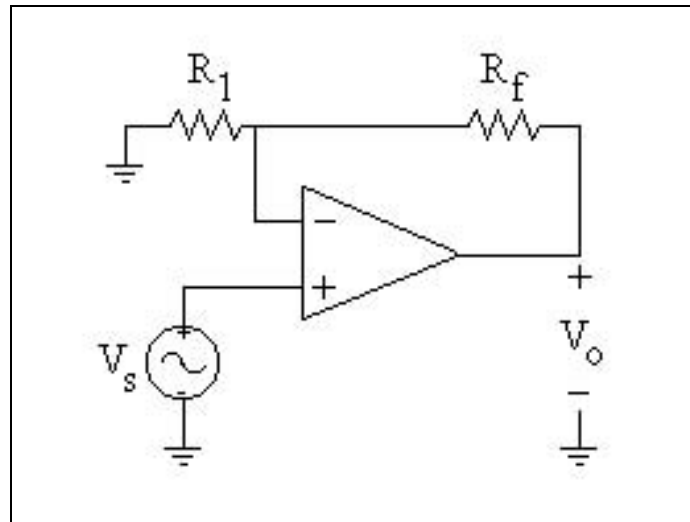
Figure 1.8: Basic Noninverting Amplifier

Setting $V^+ = V^-$, and realizing that

$$V^+ = V_{in} \tag{1.9}$$

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The simple voltage divider expression gives

$$V^- = V_{out} \frac{R_1}{R_1 + R_f} \tag{1.10}$$

Since feedback forces $V^+ = V^-$, equating the two previous expressions and solving for $\frac{V_{out}}{V_{in}}$ gives the following expression for closed loop voltage gain A_v for a noninverting amp:

$$A_v = \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_1} \tag{1.11}$$

Input Resistance

The input resistance of a circuit is given by

$$R_{in} = \frac{V_{in}}{I_{in}} \tag{1.12}$$

As we said above, the input resistance of the op-amp is extremely high. As a result, the input resistance of the noninverting amplifier is also extremely high since the input is directly into the op-amp terminal. It turns out that, due to feedback, the resistance of the noninverting amplifier is even larger than that of the op-amp by itself. The large input resistance can be verified qualitatively by placing a resistor in series between V_{in} and V^+, and determining the current that flows through it. This can be done by measuring the voltage difference on either side of the resistor, and dividing by the resistor value.

Output Resistance

We mentioned above that the output resistance of a 741 op-amp is approximately 40Ω. Feedback acts to reduce the output resistance of the circuit to virtually zero. To find the output resistance of a circuit, the output of the circuit can be thought of as a voltage source in series with an output resistor. If no load resistor is attached to the output, the output voltage will be equal to the source voltage (This source voltage is often refered to as the open circuit output voltage, why?). However, once current is drawn from the output, the output voltage will be different from the source voltage. This is described by the following equation:

$$V_{out} = V_{open} - I_{out}R_{out} \tag{1.13}$$

where V_{open} is the measured op-amp output voltage when no load resistor R_L is attached to the output ($I_{out} = 0$). By determining I_{out} for various load resistors, equation(1.13) can be used to determine the output resistance R_{out} of the circuit.

1.4.2 Inverting Amplifier

The inverting amplifier configuration is shown in Fig. 1.9.
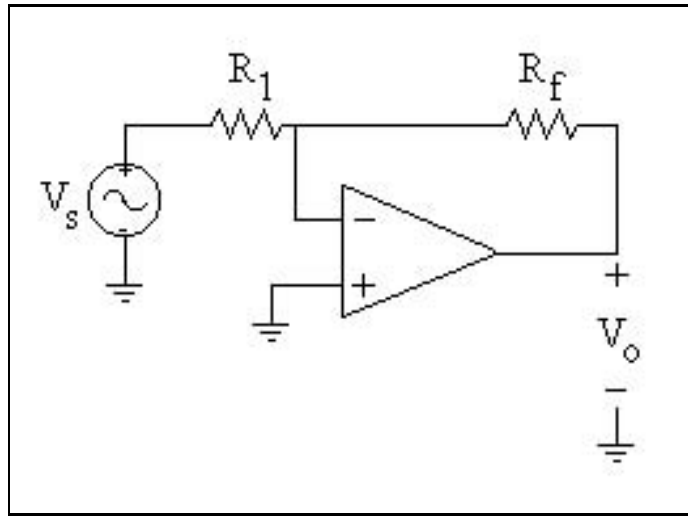
Figure 1.9: Inverting Amplifier

Equating $V^+ = V^-$ and realizing the V^+ is grounded means that $V^- = 0$. Since the ideal op-amp draws no current $(R_{in} = \infty)$, Kirchoff's laws give $I_s = -I_f$. Since $I_s = \frac{V_{in}}{R_1}$ and $I_f = \frac{V_{out}}{R_f}$, then algebra yields the inverting op-amp gain A_{inv}:

$$A_{inv} = \frac{V_{out}}{V_{in}} = \frac{-R_f}{R_1} \tag{1.14}$$

Input Resistance

The input resistance of the inverting op-amp is simply R_1. This is readily understood by applying equation (1.12) to the noninverting amp, and realizing that feedback forces $V^- = 0$.

1.4.3   Experiment on Simple Op-Amps

One of the purposes of this course is to demonstrate the utility of electronics. As a step toward this we want you to use the power supply you built in the previous experiment to power the following op-amp circuits.

(The 741 op-amps you are using have the following pin-outs: V^-, V^+, V_{out} are pins 2, 3 and 6, respectively.) To power the circuit, apply the positive side of your power supply to pin 7 of the op-amp, and the negative side of your supply to pin 4. This provides the DC bias current necessary to power the op-amp circuits you are about to build.

1. Set up your op-amp as a comparator. To do this, ground V^-, and apply the following signal to the input $V_{in} = 1.0sin(2\pi100t)$ intoV^+. Sketch the output and the input versus time.

2. Using resistors design and construct a noninverting op-amp amplifier with a voltage gain of 11 at a signal frequency of 100Hz. Set the amplitude of the input signal to

approximately 0.1V. The resistor values you use should be aimed at being appropriate for currents in the one milliamp range. (The 741 op-amps you are using have the following pin-outs: V^-, V^+, V_{out} are pins 2, 3 and 6, respectively. To power the circuit, apply the positive side of your power supply to pin 7 of the op-amp, and the negative side of your supply to pin 4. This provides the DC bias current necessary to power the op-amp circuits you are about to build. (BEFORE DOING THIS, MAKE SURE YOUR POWER SUPPLY IS WORKING PROPERLY BY SHOWING IT TO YOUR TA.)

3. After you achieve the voltage gain of 11, increase the input signal amplitude to about 2 volts. What happens? What is your maximum input voltage before clipping occurs?

4. Return the input voltage back to approximately 0.1V amplitude. Increase the frequency taking a data point at each decade starting at 100Hz, until your input signal is 1MHz. What happens to your gain as a function of frequency, do you know why?

5. Using the discussion and equations in the previous section , develop a method to to show that the output resistance of the noninverting op-amp is virtually zero. (Hint: Determine the output voltage and current for a series of load resistors ranging from 1K to 100K, and then use equation (1.13).

6. Using the discussion and equations in section , develop a method to to show that the input resistance of the noninverting op-amp is virtually infinity.

7. Using resistors, design an inverting op-amp amplifier with a voltage gain of -10 at a signal frequency of 100Hz. Steadily increase the frequency of your input signal to 1MHz, taking a data point at each decade. What happens to your gain and why?

8. Theoretically determine and also measure the input resistance of your circuit. Does your measured value agree with theory?

9. Since the output of the inverting amp looks identical to the output of the noninverting amp, its output resistance should be approximately the same, ie, virtually zero. Using methods developed above, show that this is true.

1.5   Preliminary Questions

For preparation of this lab, answer the following questions.

1. Sketch the voltage signal before and after the diode in Fig. 1.1, as a function of time. Take the input signal to be $V(t) = 3sin(2\pi 100t)$, where t is in seconds.

2. Sketch the input voltage signal and the signal across the resistor versus time for the circuit in Fig. 1.2. Take the input signal to be $V(t) = 10sin(2\pi 100t)$, where t is in seconds.

3. Sketch the voltage signals on either side of the transformer, and the signal across the capacitor versus time for the circuit in Fig. 1.3. Take the signal frequency into the transformer as 60Hz.

4. Sketch the voltage signals on either side of the transformer, and the signal across the parallel resistor-capacitor versus time for the circuit in Fig. 1.4. Take the signal frequency into the transformer as 60Hz. Calculate the AC ripple for three values of load resistors: $R_L = 5K$, $10K$, $100K$, and take the capacitor to be $2200\mu F$.

5. Sketch the voltage signals on either side of the transformer, and the signal across the parallel resistor-capacitor versus time for the circuit in Fig. 1.5. Take the signal frequency into the transformer to be $V(t) = 120\sqrt{2}sin(2\pi 60t)$, and the step-down turns ratio to be 5:1. Calculate the AC ripple for three values of load resistors: $R_L = 5K$, $10K$, $100K$, and take the capacitor to be $2200\mu F$.

6. Sketch the voltage signals on either side of the transformer, versus time for the circuit in Fig. 1.6. Take the signal frequency into the transformer to be $V(t) = 120\sqrt{2}sin(2\pi 60t)$, and the step-down turns ratio to be 5:1. Also, sketch the the signals on the two output lines.

7. Calculate the low frequency voltage gain for the circuit in Fig. (1.8). Take $R_f = 10K$, and $R_1 = 5K$.

8. Calculate the low frequency voltage gain for the circuit is Fig. (1.9). Take $R_f = 50K$, and $R_1 = 10K$.

Laboratory 2

Simple Transistor Amplifiers

2.1 Introduction

When we consider amplifiers, we are usually dealing with signals that vary in time. Generally speaking, an amplifier takes a small time-dependent signal as input and usually transforms it into a larger replica of the signal at the output. In transistor amplifier design, first a DC bias point is usually established. This point consists of the DC voltages and currents that exist within the amplifier when no input signal is applied. When a signal is applied to the input, the internal voltage levels depart from their DC operating point. The variation from this DC level gives rise to the amplification process. Simple amplifiers can be made from a single bipolar junction transistor (BJT). To understand how to do this, we will first examine the DC characteristics of a BJT and then investigate how the change from these DC conditions gives rise to amplification. To implement these circuits, you will use the NPN 2N3904 BJT, which is a general purpose transistor.

2.2 BJT Forward Active Operation, Equivalent Circuit and β

2.2.1 Theory

A silicon NPN BJT consists of a P-type silicon region sandwiched between two N-type silicon regions as shown in Fig.2.1. The P-type region, which is called the base, is very narrow. The N-type regions are called the emitter and the collector. The structure is actually two PN junctions which are in very close proximity to each other. At this point we will not concern ourselves with the physical details of how a BJT works, but we will give its equivalent circuit for amplifier operation.

To function as an amplifier, the BJT is biased to operate in what is called the forward active region. In the forward active region, the base-emitter PN junction must be forward biased, while the base-collector junction must be reverse biased. BJT operation can be fairly
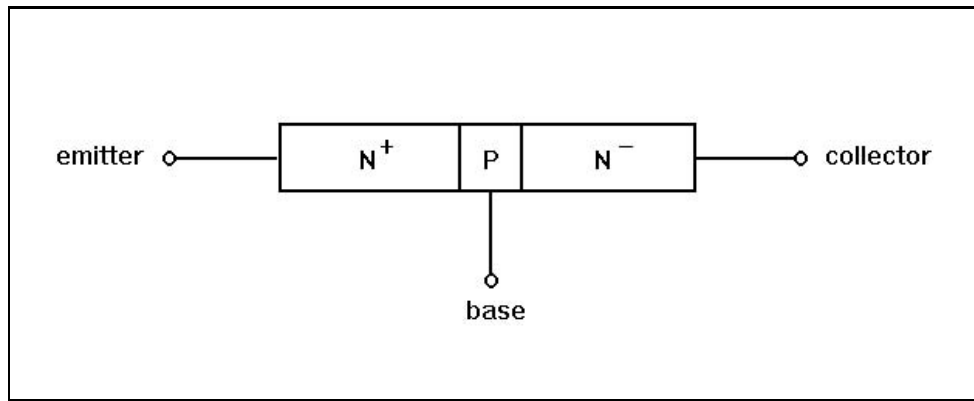
Figure 2.1: BJT Basic Structure (NPN)

complicated, but you can go very far without worrying about the details and consider a BJT in forward active to be a three-terminal device composed of a diode and a current controlled current source as shown in Fig. 2.2.
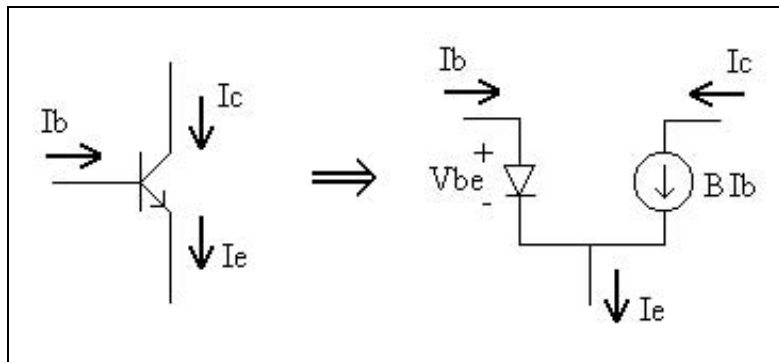
Figure 2.2: Large Signal Equivalent Circuit

Whenever we analyze or design circuits in this chapter, we will assume that the BJT operation is governed by its equivalent circuit, and analysis is performed by replacing the BJT circuit symbol on the left of Fig. 2.2 with the equivalent circuit on the right of Fig. 2.2.

The BJT then has three terminals, the base, collector and emitter, and thus three terminal currents, I_b, I_c, and I_e, which are defined in the Figure above.

In forward active, the collector current is equal to the base current times the current gain β or $I_c = \beta I_b$, where β is typically about 200, and in this course, unless otherwise noted, we will use a default value of $\beta = 200$. From Kirchoff's current law we have

$$I_e = I_c + I_b \tag{2.1}$$

Substituting $I_c = \beta I_b$ we have

$$I_e = I_b(1 + \beta) \tag{2.2}$$

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Furthermore, the base current I_b depends on the base emitter voltage V_{be}. (Note that while this expression is very accurate, it does contain approximations which will be discussed later.)

$$I_b = I_S exp \frac{V_{be}}{V_t} \tag{2.3}$$

I_S is the saturation current which is a parameter like β that depends on the specific BJT construction. Also V_t is the thermal voltage which is equal to $\frac{KT}{q}$ where K, T, q are Boltzmann's constant, absolute temperature and electron charge, respectively. At room temperature $V_t = 0.026V$.

2.2.2 DC Levels and Loop Equations

Now look at Fig. 2.3. In designing BJT circuits, it is often important to ascertain DC voltage levels at the base (V_B), emitter (V_E) and collector (V_C). For this figure, these DC levels are determined by applying the following loop equations:

$$V_B = V_{CC} - I_B R_B \tag{2.4}$$

where V_{CC} in the figure is 10V.

$$V_E = V_B - V_{BE} \approx V_B - 0.7 = I_E R_E \tag{2.5}$$

$$V_{CC} - I_B R_B - 0.7 - I_E R_E = 0 \tag{2.6}$$

Since $\beta \gg 1$, $I_E \approx I_C$, we can use the following expression for the collector voltage:

$$V_C = V_{CC} - I_C R_C \approx V_{CC} - I_E R_C \tag{2.7}$$

2.2.3 Experiment: Determining BJT Current Gain β and Verifying the Equivalent Circuit

1. Set up the circuit in Fig. 2.3. Let $R_E = 500, R_C = 500, R_B = 200K$. By measuring the voltages V_C, V_B, and V_E, and solving the appropriate loop equations, determine I_C, I_B, and I_E, respectively. Verify that $I_C \approx I_E$. From the ratio $\frac{I_C}{I_B}$, calculate β. Note that the BJT is in the forward active region. A NPN BJT is in forward active when $V_C > V_B > V_E$.

2. Change R_E to three different values. Make a table of R_E, I_B, I_C, I_E, V_{BE} and β for each value of R_E. Note that the values you choose for R_E cannot be anything, but must be chosen so that your BJT is still operating in forward active for each choice of R_E. Your data should verify that β is fairly constant and V_{BE} is approximately 0.7V (one diode drop).

3. Set R_E back to its original value of 500. Now change R_C to three different values. (Again, R_C values must be chosen to ensure you're still in forward active.) Measure I_B, I_C, I_E, and make a table to verify that I_C is approximately independent R_C. In other words, I_C should not change and the collector acts as a good current source as shown in the equivalent circuit.

4. From your data, construct an equivalent circuit for the BJT by putting in an average value for β and an average value for V_{BE} into the circuit in Fig. 2.3. Compare your extracted value of β to our default value of 200.
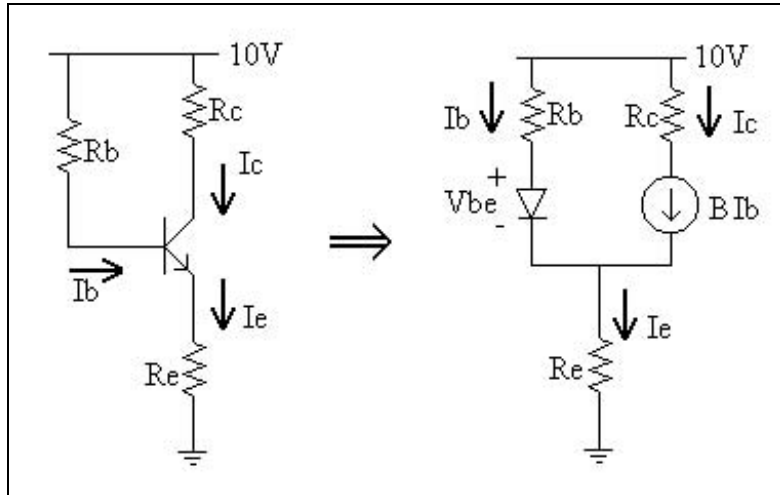
Figure 2.3: Circuit for Determining β

2.3 Common Emitter Amplifier: DC Bias

2.3.1 Theory

The circuit in Fig. 2.4 is a Common Emitter (CE) Amplifier. As discussed above, with the CE amplifier, we first use R_1, R_2, C_1, and C_2 to set up a DC operating point with $v_{in} = 0$. The purpose of C_1 and C_2 is to isolate the DC operating point currents and voltages from the rest of the world, i.e, the signal source and the load. After establishing a DC operating point, an input signal is applied to the base coupling capacitor C_1. For large enough frequencies, the signal will pass through the coupling capacitor and enter the base. This will result in variations in the bias conditions in accordance with the input signal. The variation of bias conditions at the collector is then passed through the capacitor C_2, which is taken to be v_{out}. The small signal voltage gain is then considered to be $\frac{v_{out}}{v_{in}}$.

For simple CE amplifiers, we have to first establish a DC bias condition which means that we have to choose bias resistors R_1 and R_2 that give us appropriate values for V_C, V_B
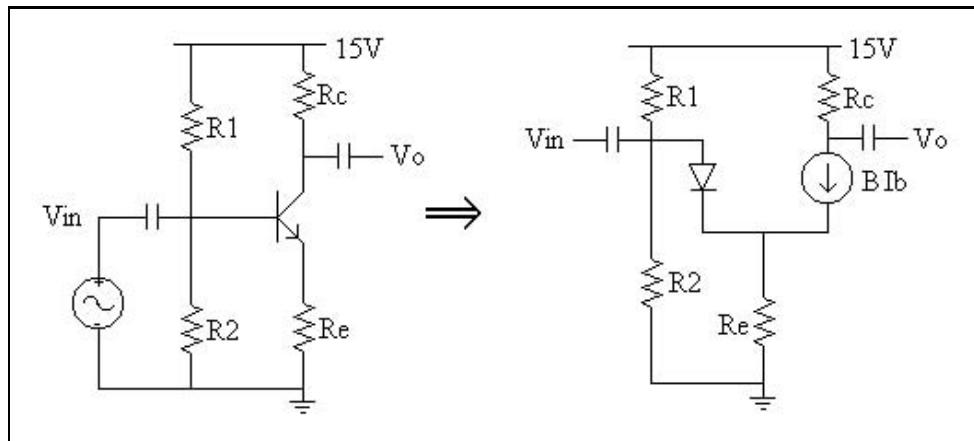
Figure 2.4: Common Emitter Amplifier

and V_E. The DC bias point is usually established to allow for a large variation or swing in v_{out}. To provide this large swing in v_{out}, a bias network is chosen so that $V_C \approx \frac{V_{CC}}{2}$. In addition, V_B and V_E are chosen to be relatively small to make sure that $V_C > V_B$ and the BJT does not enter the saturation region. (Saturation occurs when both the base-emitter and the base-collector junction are forward biased.)

If the values of R_1, R_2, R_E, R_C and V_{CC} are already known, (which is the situation for analyzing existing circuits) the DC bias conditions can be determined by first replacing the voltage divider with its Thevenin equivalent, and then by directly applying loop equations to the circuit while $v_{in} = 0$. To see this consider the circuit in Fig. 2.5.
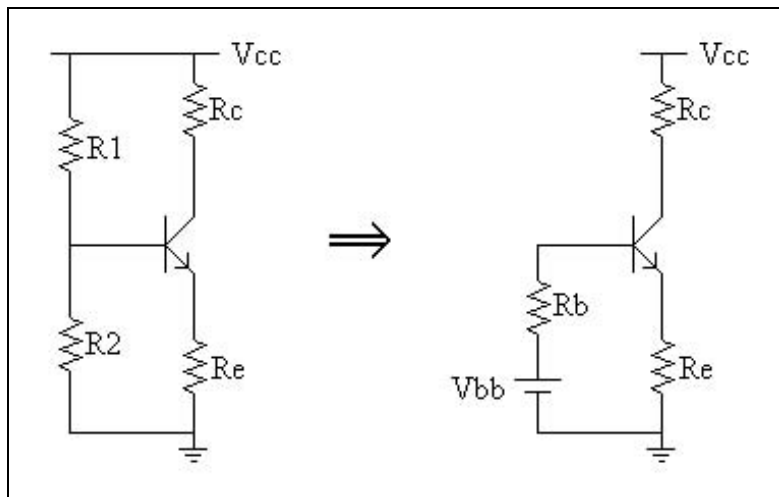
Figure 2.5: Determining DC Bias

Using KVL on the base emitter loop, we obtain

$$V_{BB} = I_B R_B + I_E R_E + V_{BE} \tag{2.8}$$

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where $R_B = R_1 || R_2$ and $V_{BB} = \frac{V_{CC}R_2}{R_1+R_2}$.

The B-E loop gives one equation and three unknowns. We can easily reduce the number of unknowns by making the very good approximations $I_C \approx I_E$, and $V_{BE} = 0.7V$. Using these approximations and recalling that $\beta I_B = I_C$, we can obtain the following equation for I_C in terms of known parameters.

$$I_C = \frac{V_{BB} - 0.7}{\frac{R_B}{\beta} + R_E} \tag{2.9}$$

With I_C determined, V_C and V_E are readily obtained by observing that:

$$V_C = V_{CC} - I_C R_C \tag{2.10}$$

$$V_E = I_E R_E \tag{2.11}$$

$$V_B = V_E + 0.7 \tag{2.12}$$

2.3.2   Experiment: CE Amp DC Bias

1. Set up the circuit in Fig. 2.6 with $V_{CC} = 15V$.

2. Use the preceding equations to theoretically determine V_C, V_B, V_E. and I_C, I_E.

3. Measure the voltages at V_C, V_B and V_E. and then determine I_C, I_B, and I_E.

4. Compare the measured and calculated values.
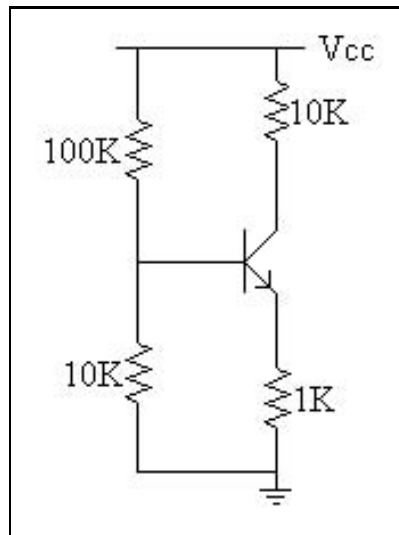
Figure 2.6: CE Amp for DC Bias Experiment

2.4   CE Amp Small Signal Voltage Gain at Midband Frequencies

2.4.1   Theory: Approximate Analysis

In this chapter, we will only consider operation at frequencies large enough where coupling capacitors C_1 and C_2 can be approximated to be short-circuits. Furthermore, we will not consider frequencies which so high that the intrinsic capacitances of the BJT itself affect circuit performance. These capacitances will be treated in another lab. Thus we will only be considering circuit performance for these midband frequences which for BJT circuits typically range from 10kHz to 1MHz.

Having defined our region of frequency operation, let's get back to amplifiers. As mentioned above the CE configuration is useful for amplifying small signal voltages. To understand this refer to Fig. 2.4 and the following discussion. Recall that a small change in base current leads to large change in collector current. Now, this small change in base current can be achieved by applying a small AC voltage to the base, which in turn will give rise to a large change in collector current so that $\Delta I_c = \beta \Delta I_b$. It follows that when a relatively large resistor R_C is placed between the power supply V_{CC} and the collector, the voltage variation across R_C and thus the voltage variation at the collector, due to the large change in collector current, will also be large. Thus, a small change in base voltage can lead to a large change in collector voltage. If we consider the input signal to be the change in base voltage, and the output signal to be the change in collector voltage, then the voltage amplification or gain will be $A_v = \frac{v_{out}}{v_{in}} = \frac{\Delta V_c}{\Delta V_b}$. By choosing the appropriate resistor values, we can design a simple CE amplifier with the voltage gain we want. To understand this, consider the following example. Recall, the voltage gain is $A_v = \frac{v_{out}}{v_{in}} = \frac{\Delta V_c}{\Delta V_b}$. The general procedure will be to find V_c and V_b from simple applications of Kirchoff's laws, and then find the small or incremental changes in these voltages due to an applied signal at the base.

Using KVL directly on the base emitter loop, and recalling that for most BJT's $I_e \approx I_c$, and thus substituting I_e for I_c, gives

$$V_b = I_c R_E + V_{be} \tag{2.13}$$

If we make an incremental change in V_b by applying a small signal to the base we obtain:

$$\Delta V_b = \Delta I_c R_E + \Delta V_{be} \tag{2.14}$$

At this point we could continue our analysis in detail to determine ΔV_{be}. However, it is useful to use our knowledge of diodes and BJT's to get some insight. Recall, the relationship between I_c and V_{be} is exponential. In other words, a small change in V_{be} leads to a large change in I_c. Furthermore, once a silicon diode turns on, its voltage drop will not change much from its DC value of $\approx 0.7V$. Thus ΔV_{be} is almost always very small. Therefore, a zero order approximation can often be made to neglect ΔV_{be} compared with $\Delta I_c R_E$ to yield:

$$\Delta V_b \approx \Delta I_c R_E \tag{2.15}$$

Now let's look at the collector voltage V_C. From KVL we have

$$V_c = V_{CC} - I_c R_C \tag{2.16}$$

Since V_{CC} represents a DC power supply $\Delta V_{CC} = 0$, therefore making an incremental change in V_c leads to the following relationship:

$$\Delta V_c = -\Delta I_c R_C \tag{2.17}$$

Taking the ratio $\frac{v_{out}}{v_{in}} = \frac{\Delta V_c}{\Delta V_b}$ for the voltage gain yields:

$$\frac{v_{out}}{v_{in}} \approx -\frac{R_C}{R_E} \tag{2.18}$$

Equation 2.18 shows that the approximate voltage gain of the CE amp is simply the ratio of the collector resistor to the emitter resistor. It's amazing how far you can get with this simple result.

2.4.2   Experiment

1. To the circuit you already built in Fig. 2.6, add capacitors to the input and output as shown in Fig. 2.7.
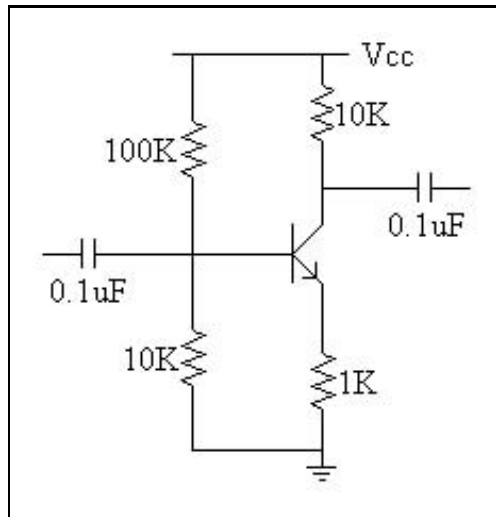
Figure 2.7: CE Circuit for small signal gain

2. Apply an input signal to the circuit as shown in Fig. 2.7. For v_{in} use a 0.1V, 100KHz signal from your wavetek. Determine the voltage gain. Sketch v_{out} versus v_{in}.

3. Increase the input signal amplitude until the output gets clipped. This clipping represents distortion which usually means that the output signal is not an exact replica of the input. The output amplitude right before clipping occurs is called the swing of the amplifier. What is the swing of your circuit? Why does clipping occur?

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4. Replace R_C with a 5K resistor and determine the voltage gain and swing.

5. Design: Choose a new value for R_C to give a voltage gain of approximately $-7V/V$. What is the swing of your new amp?

2.4.3 Theory: Accounting for V_{be} in the CE Amp

Often in CE amps, R_E is small or even zero. Under these circumstances, the effect of ΔV_{be} can not be neglected in small signal analysis. To account for ΔV_{be} in our expression for voltage gain, we have to express it in terms ΔI_c as well as known quantities. To do this we go back to our original expression relating V_{be} and I_c.

$$I_c = \beta I_s e^{\frac{V_{be}}{V_T}} \tag{2.19}$$

Using Taylor series we can obtain the small signal change in I_c that results in a small change in V_{be}.

$$\Delta I_c = \frac{\partial I_c}{\partial V_{be}} \Delta V_{be} \tag{2.20}$$

Performing the differentiation and using 2.19, leads to

$$\Delta I_c = \frac{I_C}{V_T}|_{I_C} \Delta V_{be} \tag{2.21}$$

Usually, $\frac{\partial I_c}{\partial V_{be}}|_{I_C}$ is defined as the small signal transconductance of the BJT, which is designated as g_m. It is important to note that g_m is given for a specific I_C which is determined by the DC bias condition. Thus, the transconductance is given by

$$g_m = \frac{\partial I_c}{\partial V_{be}}|_{I_C} = \frac{I_C}{V_T} \tag{2.22}$$

and the small signal change in V_{be} is

$$\Delta V_{be} = \frac{\Delta I_c}{g_m} \tag{2.23}$$

Now, if we substitute $\frac{\Delta I_c}{g_m}$ for ΔV_{be} in Equation (2.14), and take the ratio $\frac{\Delta V_c}{\Delta V_b}$, we find that the voltage gain, while including the effect of ΔV_{be}, is:

$$A_V = \frac{v_{out}}{v_{in}} = \frac{\Delta V_c}{\Delta V_b} = \frac{-R_C}{\frac{1}{g_m} + R_E} \tag{2.24}$$

Now, if R_E were to be totally eliminated from the circuit, then we could just set $R_E = 0$ in the above equation, and the gain would become:

$$A_V = -g_m R_C \tag{2.25}$$

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2.4.4   Experiment

1. Determine the value of g_m and theoretically calculate the voltage gain using Equation (2.25). Compare your results with the theoretical results. Does inclusion of ΔV_{be} give results which are in better agreement with experiment?

2. Build the circuit in Fig. 2.8.
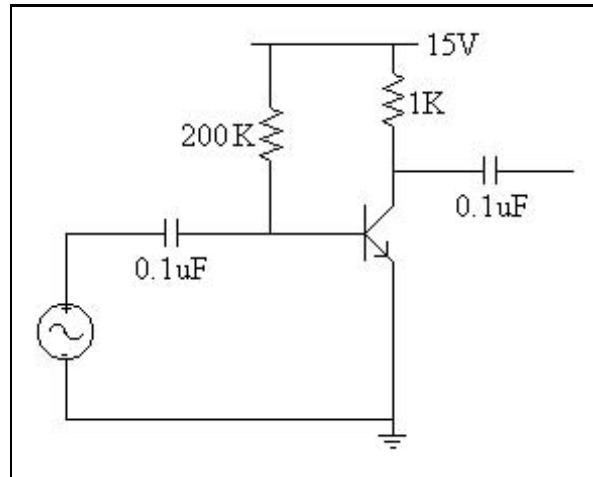
Figure 2.8: CE Amp with $R_E = 0$

Notice that the 200K resistor provides the base current necessary for establishing a DC bias.

3. Measure the DC voltages to make sure the BJT is in the forward active region. If it's not in forward active, adjust your resistor values to compensate.

4. Perform a small signal theoretical analysis to predict what the voltage gain of the circuit should be.

5. Measure the voltage gain. Adjust the input signal from your wavetek to approximately 10mV amplitude, with a frequency of 100kHz. What is the voltage swing? (If your signal source cannot reach as low as 10mV, you can use a simple voltage divider to achieve the required level.)

6. Do the measured values for gain and swing agree with your theoretically predicted ones to within 25% error, why or why not?

7. Design: Theoretically determine what new value of R_C you need to reduce the gain by 50% of what your measure above. What is the new swing.

8. Substitute this new value of R_C and measure the gain and the swing. Does the values agree with your theoretically predicted values to within 25% error?

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2.4.5 Theory: Voltage Amplifier Equivalent Circuit, Input Resistance and Output Resistance

Input Resistance:

The input resistance is the resistance seen by the current source or voltage source which drives the circuit. For example, returning to the circuit in Fig. 2.7, the impedance seen by sinusoidal input signals looking into the capacitor is:

$$Z_{in} = \frac{1}{j\omega C_1} + R_B || R_{TB} \tag{2.26}$$

Where R_{TB} is the resistance looking into the base of the transistor. As we have done throughout this lab, let's consider only cases where the frequency is large enough that the impedance of the capacitor can be ignored. We call these frequencies the midband range. At midband, the input impedance can be approximated as the following input resistance.

$$R_{in} = R_B || R_{TB} \tag{2.27}$$

R_B can be read directly from the circuit. However, we must determine R_{TB}. The resistance seen looking into the base can be determined by grounding the output, and then applying a small signal to the base ΔV_b, and determining the base current that is drawn ΔI_b. The ratio of the small signal base voltage to the small signal base current is then R_{TB}. To determine R_{TB}, let's first make the excellent approximation that $I_c = I_e$, and use Eqns. (2.14) and (2.23) to obtain:

$$\Delta V_b = \frac{\Delta I_c}{g_m} + \Delta I_c R_E \tag{2.28}$$

Now, recalling that $\Delta I_b = \frac{\Delta I_c}{\beta}$, and dividing ΔV_b by ΔI_b, we obtain

$$R_{TB} = \frac{\Delta V_b}{\Delta I_b} = \frac{\beta}{g_m} + \beta R_E \tag{2.29}$$

Since $\frac{1}{g_m}$ is usually much smaller than R_E, when an emitter resistor is present a good approximation for the input resistance is simply βR_E. Of course, when the emitter is connected directly to ground, $R_E = 0$ and under these circumstances $R_{TB} = \frac{\beta}{g_m} = r_\pi$ Note, that we have followed the customary convention and defined $\frac{\beta}{g_m}$ to be r_π.

It is interesting to observe that the resistance looking into the base is usually fairly large since it contains the multiplicative factor β. This can be explained because the current actually entering the base is I_b, while the current through R_E is approximately βI_b. This can alternatively be viewed as I_b going through an effective resistance of βR_E, thus giving the impression of a much larger resistance.

Output Resistance

Output resistance is an indication of a source's ability to drive a load impedance. An ideal voltage source has zero output resistance, and an ideal current source has infinite output resistance. To find the output resistance of the CE amplifier, we ground the input and drive the output. From the circuit in Fig. 2.7, the output resistance is then $R_C || R_{TC}$, where R_{TC} is the resistance looking into the collector. Since, at this time, we are considering the collector to be modeled as an ideal current source, the output resistance of the CE amp is then simply R_C.

Voltage Amplifier Equivalent Circuit

Now that we have determined the voltage gain, as well as the input and output resistances of the CE amp, it can be represented as a simple two-port circuit in Fig 2.9 The nice thing about this equivalent circuit is that once it's established, you don't have to worry about the details of the circuit operation, but can just treat it as a black box with a specific open circuit output voltage, an input resistance and an output resistance. We can therefore write the CE amp at midband frequencies as a black box with $R_{in} = (r_\pi + \beta R_E) || R_B$; $R_{out} = R_C$; and the open circuit output voltage given by $v_{out} = A_V v_{in}$.
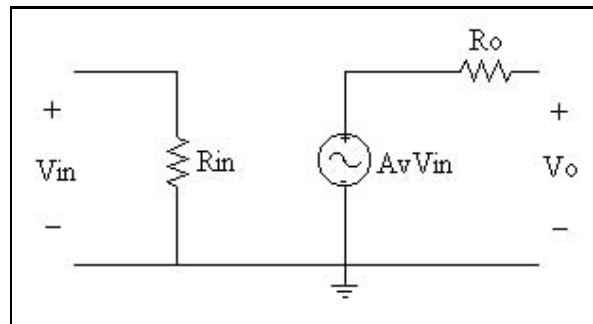
Figure 2.9: Two-Port Equivalent Amplifier Circuit

Example:

To appreciate the usefulness of the two-port amplifier equivalent circuit, consider the following example. Suppose you have a CE amp that is driven by a voltage source with source resistance R_S, and the amp is supplying current to a load R_L. The actual circuit is drawn below.

If we replace the small signal part of the CE amp with its two-port amp equivalent circuit, we obtain the small signal equivalent amplifier circuit shown in Fig. 2.11.

We can easily find the voltage gain by dividing the circuit into three stages and finding the gain of each stage. The total gain is then the product of the three individual stage gains.

The first stage is just the voltage divider consisting of v_S, R_S, and R_{in}.

$$A_{V1} = \frac{v_1}{v_s} = \frac{R_{in}}{R_S + R_{in}} \tag{2.30}$$

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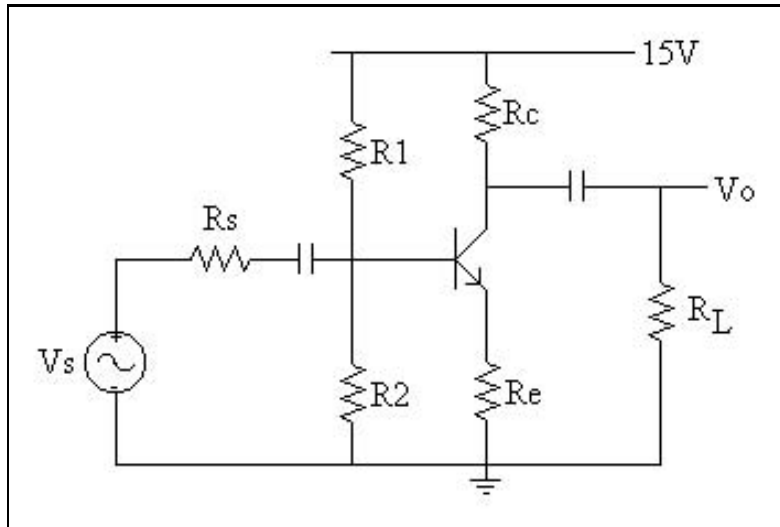
Figure 2.10: CE amp driven by nonideal source of resistance R_S and driving a load R_L
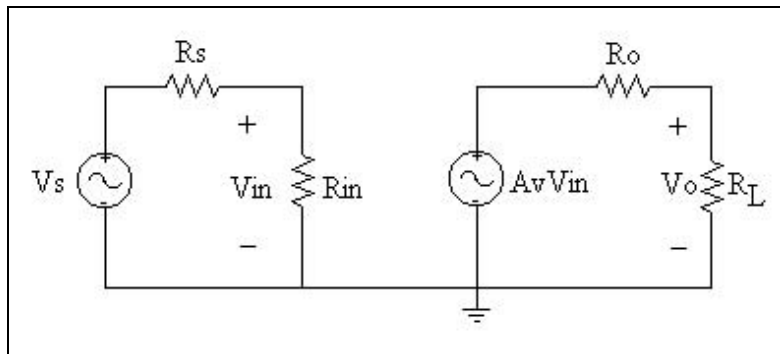
Figure 2.11: Equivalent circuit of CE amp described by voltage amplifier

Where V_1 is the voltage seen at the input of the CE two-port amp equivalent circuit.

   The second stage is the CE two-port amp equivalent circuit.

$$A_{V2} = \frac{V_2}{V_1} = \frac{-R_C}{\frac{1}{g_m} + R_E} \tag{2.31}$$

Where V_2 is the open circuit voltage at the CE amp output that would be measured if the load R_L were not there.

   The final stage is the voltage divider consisting of V_2, R_{out}, and R_L.

$$A_{V3} = \frac{v_{out}}{V_2} = \frac{R_L}{R_L + R_{out}} \tag{2.32}$$

Finally, the total gain of the circuit A_V is the product of the three stages:

$$A_V = \frac{v_{out}}{v_s} = A_{V1}A_{V2}A_{V3} = \left(\frac{R_{in}}{R_S + R_{in}}\right)\left(\frac{-R_C}{\frac{1}{g_m} + R_E}\right)\left(\frac{R_L}{R_L + R_{out}}\right) \qquad (2.33)$$

2.4.6 Experiment: Effect of Input and Output Resistances

1. Construct the circuit in Fig. 2.10. Notice that it is really just the CE amp of Fig. 2.6, driving a load of $R_L = 1K$, and being driven by a voltage source with source resistance $R_S = 10k$.

2. Using the expressions above, theoretically determine the voltage gain of the circuit.

3. Measure the voltage gain $\frac{v_{out}}{v_s}$ under the same input voltage and frequency conditions as in Exp. 2.4.2. Compare the measured gain with your theoretical result.

4. Try two different values for the load resistor: let $R_L = 5K$ and $R_L = 10K$. From the output voltages measured for the different values of R_L determine the output resistance of the CE amp R_{out}. Compare the value with the theoretical one.

5. Replace R_L with its original value of $1K$. Now, measure the AC voltage at the base. Now repeat your measurement with two different values for the source resistor: let $R_S = 5K$ and $R_S = 10K$. From the base voltages measured for the different values of R_S determine the input resistance of the CE amp R_{in}. Compare the value with the theoretical one.

2.5 Emitter Follower

The emitter follower (EF) configuration is shown in Fig. 2.12.

The EF amp has a voltage gain of approximately one. With this kind of gain, you may ask what is the point? The point is that an EF has a very low output resistance and a high input resistance. It is therefore used as a buffer which is placed in between a high resistance source and a low resistance load, thereby providing the necessary current to the load without sagging the voltage. This will become more clear after this part of the experiment.

2.5.1 Theory: DC Bias and Small Signal Voltage Gain

DC Bias

The DC bias for a stand alone EF amp is similar to the CE amp, but, since the gain is one, you would establish a quiescent or DC bias point so that $V_B \approx \frac{V_{CC}}{2}$, $V_C = V_{CC}$, and $V_E = V_B - 0.7V$. Recall that the $0.7V$ reflects a diode drop across the base-emitter junction.
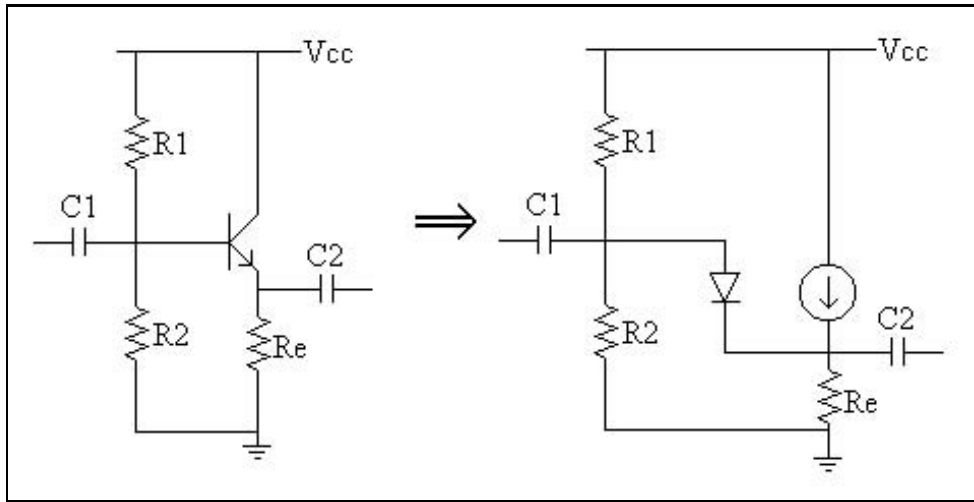
Figure 2.12: Emitter Follower Circuit

Voltage Gain

From Fig. 2.12 we see that the input is into the base (just as with the CE amp), but the output is at the emitter. We can thus use our knowledge of BJT's to immediately see that the voltage gain of an EF amp is approximately 1, Since the emitter voltage is always approximately 0.7V below the base voltage, if a small signal is appled to the base, then you will see that same signal at the emitter, just offset by 0.7V. Since the voltage gain actually reflects the change of voltage, and since the change at the base and emitter are approximately the same, the voltage gain is approximately one. To see this analytically, substitute the BJT with its equivalent circuit as shown above. First perform the base-emitter loop analysis.

$$V_b = V_{be} + I_e R_E \tag{2.34}$$

$$V_e = I_e R_E \tag{2.35}$$

Providing a small signal input leads to the following:

$$v_{in} = \Delta V_b = \Delta V_{be} + \Delta I_e R_E \tag{2.36}$$

$$v_{out} = \Delta V_e = \Delta I_e R_E \tag{2.37}$$

Taking the ratio of v_{out} to v_{in}, and recalling that $\Delta V_{be} = \frac{\Delta I_e}{g_m}$, we obtain for the gain

$$A_V = \frac{v_{out}}{v_{in}} = \frac{R_E}{\frac{1}{g_m} + R_E} \approx 1 \tag{2.38}$$

Finally, since ΔV_{be}, is usually much smaller than $\Delta I_e R_E$, the voltage gain of an EF amp can often be approximated as one.

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Input Resistance

From the input, the EF amp and the CE amp look identical. (This is actually an approximation, which we will examine later in the course.) Thus the input resistance of the EF amp and CE amp are considered the same and given by $R_{in} = R_B || R_{TB}$ where R_{TB} is the resistance looking into the base:

$$R_{TB} = r_\pi + \beta R_E \qquad (2.39)$$

Since the input resistance contains this multiplicative β factor, it is usually fairly large which is usually desirable for a voltage amp.

Output Resistance R_o

The output resistance of an EF amp is low which is usually desirable for voltage amplifiers. To find an analytical expression for the output resistance, we drive the output with a test voltage and determine the current that is drawn, while the input is shorted. The ratio of the test voltage to drawn current is the output resistance.

To find R_o consider the circuit in Fig. 2.13, which is our EF amp driven by a voltage source V_s with source resistance R_S.
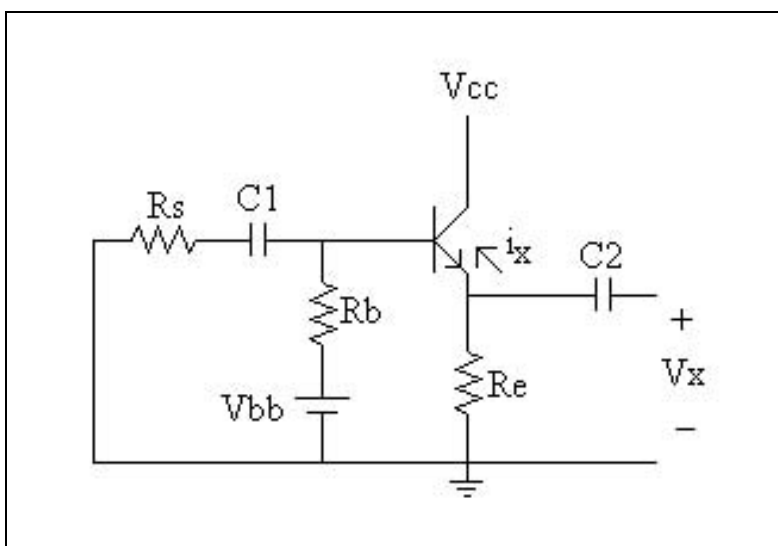
Figure 2.13: Circuit for theoretically determining R_o of EF amp.

Let's set $v_s = 0$, and drive the output with voltage v_x. The resistance v_x sees is $R_o = R_E || R_{TE}$, where R_{TE} is the resistance seen looking into the emitter. Recall, that the emitter is the n-side of a forward biased pn junction, and thus offers little resistance. Performing the emitter-base loop analysis gives

$$v_x = \Delta V_e = -\Delta V_{be} - \Delta I_b(R_B || R_S) \qquad (2.40)$$

$$i_x = -\Delta I_e = -\beta \Delta I_b \qquad (2.41)$$

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Where i_x is the small signal current going into the emitter of the BJT. Dividing v_x by i_x gives

$$R_{TE} = \frac{v_x}{i_x} = \frac{r_\pi + R_S || R_B}{\beta} \tag{2.42}$$

Thus, the output resistance is usually fairly small since it contains a division by β.

2.5.2 Experiment

1. Set up the EF circuit of Fig. 2.12 using the following values $R_1 = 10K$, $R_2 = 10K$, $R_E = 10K$, $C_1 = 0.1\mu f$, $C_2 = 0.1\mu f$.

2. Theoretically calculate the voltage gain, the input resistance and the output resistance.

3. Set the waveform generator to 100KHz, and measure the voltage gain.

4. Place a 1K source resistor between the signal generator and C_1. Now measure the gain as well as the signal voltage at the base. Trade the 1K for a 10K resistor and repeat your measurements. From your measurements determine the input resistance of the circuit.

5. With the source resistor still in place, place a 10K load resistor at the output from C_2 to ground. Measure the voltage gain. Repeat your measurements with 1K and 500Ω load resistors. From your measurements, determine the output resistance of the circuit.

6. Compare your measured results with the theoretical calculations, Does the experiment help describe the utility of the EF amp? To help understand this, consider what would have happened to the signal if the EF were not there, and the 1K load were attached directly from R_S to ground?

2.6 Putting it All Together: Practical Amplifier Design

As we mentioned above, a good voltage amplifier will have high input resistance and low output resistance. To achieve this we can combine the beneficial attributes of a CE amp with those of an EF amp by cascading CE and EF stages as shown below.

The circuit above is a two-stage amplifier. The first stage is a CE amp which provides voltage gain and relatively high input resistance. The second stage consists of an EF amp which provides low output resistance, and thus ability to drive a load without sacrificing gain.
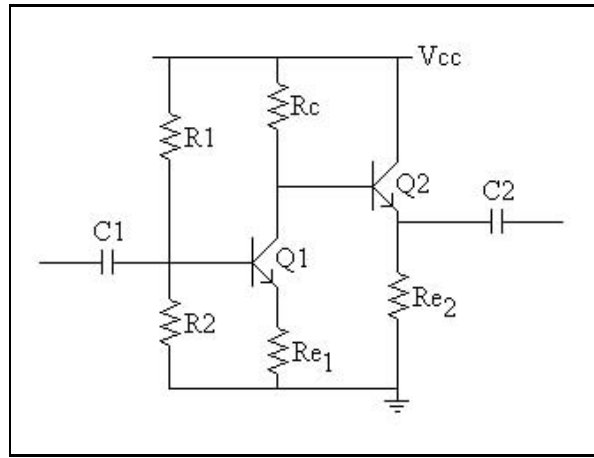
Figure 2.14: Two Stage Amplifier

DC Bias

The CE amp is biased by the voltage divider consisting of R_1 and R_2. The EF amp is biased by the collector voltage of Q_1. The main thing to understand for easily determining the DC bias of this circuit is that due to β multiplication, usually I_{B2} is negligible compared to I_{C1} and can be neglected when calculating V_{C1}. Once this approximation is made, the CE amp can be biased using the procedure identical with the one we used in Section 2.3 for the single transistor CE amp, without worrying about the EF amp. Once V_{C1} is established, the bias of the EF amp is then immediately determined by assuming $V_{B2} = V_{C1}$: then $V_{E2} = V_{B2} - 0.7$, and of course $V_{C2} = V_{CC}$.

Using the information above, determine the values of the DC voltages V_{C1}, V_{B1}, V_{E1}, V_{B2}, V_{E2}, and V_{C2}.

Small Signal Voltage Gain, Input and Output Resistance

Calculating the gain of this circuit is extremely simple. Generally, the total gain is the product of the gains of the individual stages. The only extra thing to remember is the load for the CE stage is the input resistance of the EF stage.

Determining the input resistance is simple. Since the input into the circuit looks identical to that of a simple one stage CE amp, R_{in} of the two stage amp is identical to that of the one stage CE amp of Part 2.4. Thus $R_{in} = (r_\pi + \beta R_E)||R_B$.

The output resistance is the same form as that of the EF amp of Part 2.5, with R_{C1} playing the role of R_S and $R_B = \infty$.

2.6.1 Experiment: Multi-Transistor Amplifier

1. Construct the multi-stage amplifier circuit in Fig. 2.14. Use $R_1 = 100K$, $R_2 = 10K$, $R_C = 10K$, $R_{E1} = 1K, R_{E2} = 10K$. Using the information above, determine the

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values of the DC voltages V_{C1}, V_{B1}, V_{E1}, V_{B2}, V_{E2}, and V_C.

2. Measure the DC values V_{C1}, V_{B1}, V_{E1}, V_{B2}, V_{E2}, and V_C. Compare your measured values with the calculated ones.

3. Theoretically calculate the small signal gain of the circuit

4. Input a 100kHz signal with amplitude of 0.1V into the circuit and measure the voltage gain. Compare the measured value with one you calculated above.

5. Now, add a load resistor $R_L = 10K$ and measure the gain again. How would the gain change if the second stage were not there?

2.7 Preliminary Questions

Before performing the lab, answer the following questions. Assume you are using a 2N3904 BJT, which has $\beta \approx 200$.

1. For the circuit in Fig. (2.3), calculate V_B, V_C and V_E if $V_{CC} = 10V$, $R_B = 83K$, $R_C = 500$, $R_E = 100$ and $\beta = 100$

2. For the circuit in Fig. (2.6) calculate V_B, V_C and V_E if $V_{CC} = 15V$.

3. For the circuit in Fig. (2.7), calculate the small signal voltage gain, the input resistance and the output resistance. Let $V_{CC} = 15V$.

4. What happens to the gain of the circuit in Fig. (2.7) if it is driven by an AC source with source resistance of 10K.

5. What happens to the gain of the circuit in Fig. (2.7) if it drives a load of 20K connected to the output.

6. For the multi-stage amplifier circuit in Fig. 2.14. Let $R_1 = 150K$, $R_2 = 15K$, $R_C = 20K$, $R_{E1} = 2K$, $R_{E2} = 15K$. Determine the values of the DC voltages V_{C1}, V_{B1}, V_{E1}, V_{B2}, V_{E2}, and V_C. What is the AC voltage gain? If a 20K load is attached to the output, what is the voltage gain?

Laboratory 3

Design and Build Your Own Compact Disk Hi Fi Audio System

3.1 Introduction

In the last two labs we were learning and reviewing many of the fundamentals of electronic circuit analysis. In this lab we'll try to put these basics together, along with a few new ideas to have fun building a fairly high-quality audio amplifier for a compact disc player. The main goal in making the CD audio amp is to take a relatively small signal from the CD player ($V_S \approx 0.5V$), with relatively high source resistance ($R_S \approx 1K$), and amplify it sufficiently to drive a speaker, which is usually described as an 8Ω load. A good quality amp will be able to deliver five to ten watts average power to the load, without distorting the original signal. In other words, the signal supplied to the speaker (load) should be an exact replica of the original signal coming from the CD player. Therefore, the hi-fi will amplify all frequencies equally over the audio range which is 20Hz to 20kHz. Any unwanted deviation from the original signal is considered distortion. To achieve this audio amps usually have two basic stages: (1) a pre-amp stage which increases the voltage of the original signal and (2) a current or power amp stage which makes sure the amp can source enough current so the load does not sag the voltage at the output. There are also peripherals such as tone control circuits, and of course the audio amp requires a strong enough power supply to power the circuit.

3.2 Design Considerations

3.2.1 Power to Load

To deliver the desired power to the 8Ω load we will have to determine the amount of current and/or voltage we need at the load. Recall that the expression for average power is

$$P_L = \frac{1}{T} \int_0^T V(t)I(t)dt \tag{3.1}$$

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If we take our signals to be sinusoidal, then the integral leads to the following expression for power dissipated in the speaker:

$$P_L = \frac{V_o^2}{2R_L} \tag{3.2}$$

where V_o is the amplitude of the signal and R_L is the resistance of the speaker. $R_L = 8\Omega$. Using the above expressions, we find that to deliver 6 watts to an $R_L = 8\Omega$ speaker, we require to drive the load by a sinusoidal voltage with amplitude of approximately 10V.

3.2.2 Complementary Symmetry Power Amplifiers

In most applications where AC power is driving a load, a complementary symmetry (push-pull) power amplifier is employed. This amplifier usually has a voltage gain of one, and a large current gain. It is the most efficient configuration for transforming DC power from the power supply to the AC power driving the load.

A basic complementary symmetry BJT power amplifier is shown in Fig. 3.1
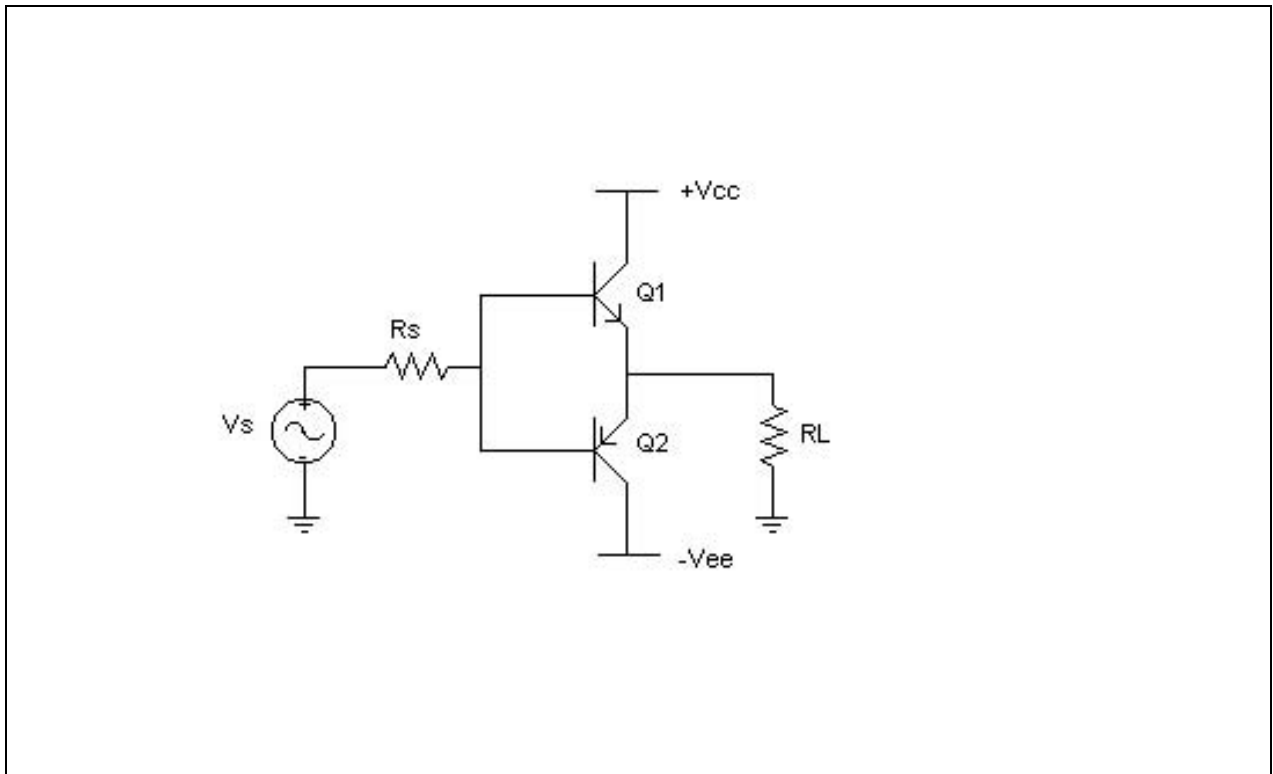

Figure 3.1: Basic Complementary Symmetry Power Amp

The BJT's provide a current gain of β, and a low output resistance. When the input is positive and greater than 0.7V, the npn BJT is on and the pnp is off. Under these conditions, the npn acts like an emitter follower, taking the input current from the base, multiplying it

by β, to provide current and a low source resistance to drive the load. Of course the extra current derived from the β multiplication has its origin at the positive DC power supply.

When the input voltage is less the -0.7V, the npn is off and the pnp is on. Under these conditions, the pnp acts like an emitter follower, taking the input current from the base, multiplying it by β, to sink current and provide a low source resistance to sink the load. Here, the extra current required by β multiplication has its origin at the negative DC power supply.

The output resistance R_{out} is given by the parallel output resistance of the npn and the pnp ($R_{on}||R_{op}$). For the positive side of the cycle, since the pnp is off, $R_{op} = \infty$. So under these conditions the output resistance is just that of the npn which is

$$R_{out} = R_{on} \approx \frac{1}{g_{mn}} + \frac{R_S}{\beta_n} \qquad v_{in} > 0.7 \tag{3.3}$$

During the negative cycle $R_{on} \approx \infty$, which yields the following for the negative cycle output resistance:

$$R_{out} = R_{op} \approx \frac{1}{g_{mp}} + \frac{R_S}{\beta_p} \qquad v_{in} < -0.7 \tag{3.4}$$

Where g_{mn}, g_{mp}, β_n and β_p are the small signal transconductances and current gains of the the npn and pnp BJT's respectively. (Note the approximation sign. This is because, strictly speaking, we are not dealing with small signals so using a single value of g_m is only an approximation.)

To appreciate how power is converted from supply by the circuit, consider the following. Each power supply provides current during only half the cycle. During the positive cycle, the positive DC supply is sourcing current, while during the negative part of the cycle the negative DC supply is sinking current. Therefore, the average current provided by the positive supply is

$$I_{+supply} = \frac{1}{T} \int_0^{T/2} I_c(t) dt \tag{3.5}$$

which for a sinusoidal waveform gives

$$I_{+supply} = \frac{I_o}{\pi} = \frac{V_o}{\pi R_L} \tag{3.6}$$

During the negative part of the cycle, a totally analogous analysis applies, but for the negative supply current $I_{-supply}$. to give the same result.

The average power for the total cycle is then obtained by adding the power from each half cycle:

$$P_{supply} = V_{CC}I_{+supply} + V_{EE}I_{-supply} \tag{3.7}$$

Since we take the magnitudes of the DC supplies to be equal, we have

$$P_{supply} = 2V_{CC}I_{+supply} = \frac{2V_{CC}V_o}{\pi R_L} \tag{3.8}$$

The power conversion efficiency η, which gives a measure of how well power is transferred from the supply to the load, is given by the ratio of the power to the load P_L to the power provided by the supplies P_{supply}:

$$\eta = \frac{P_L}{P_{supply}} = \frac{\pi V_o}{4 V_{CC}} \tag{3.9}$$

Thus, for full swing $V_o \approx V_{CC}$, the power conversion efficiency of the complementary symmetry reaches is maximum value of approximately 75%. This number is much greater than that of the single ended emitter follower that we discussed earlier.

You may have noticed that the complementary symmetry configuration has a small problem which is that no signal can propagate when $-0.7 < V_s < 0.7$ because both BJT's are off at this time. This region is often referred to as the cross-over region between the npn and pnp cycles. Hence, the accompanied distortion that results is often referred to as cross-over distortion. To avoid cross-over distortion, circuit designers often bias the two transistors slightly into the forward active region with diodes. For example, look at the circuit in Fig. 3.2.
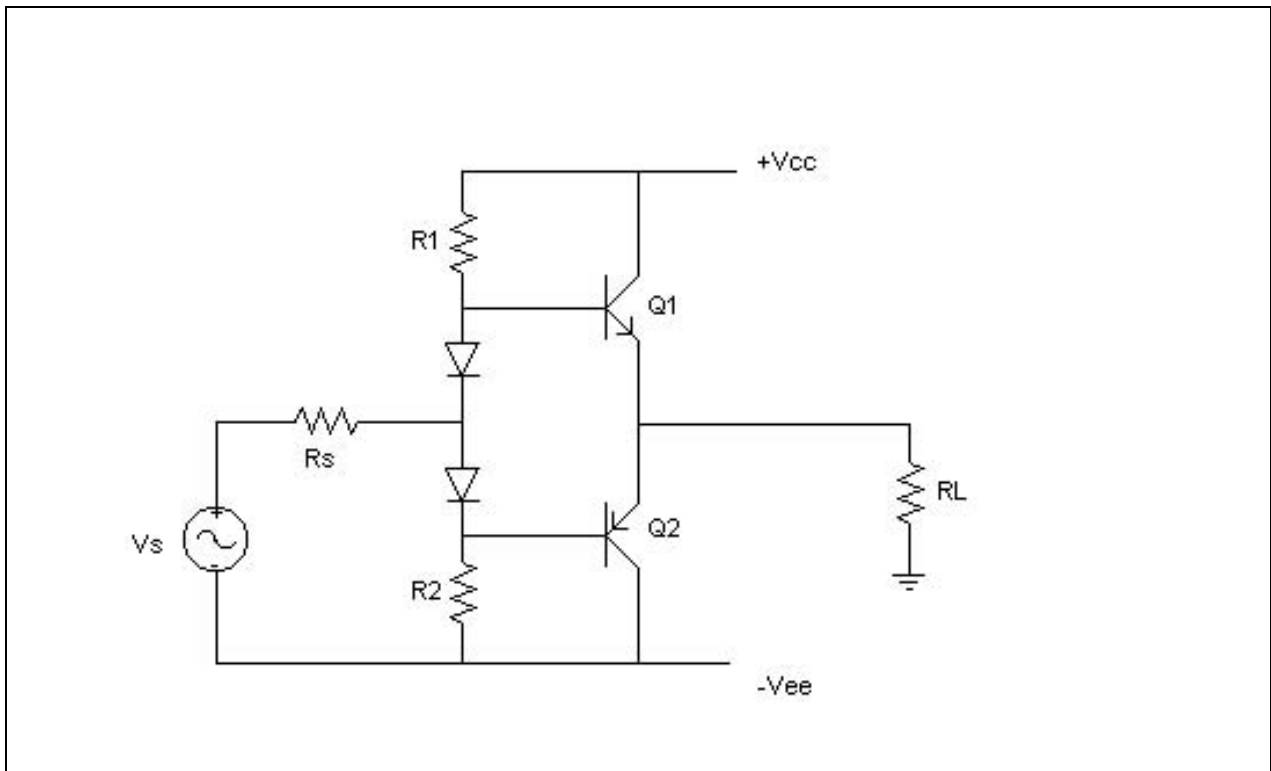

Figure 3.2: Complementary Symmetry Amp Biased to Eliminate Cross-Over Distortion

The diodes, in conjunction with resistors R_1 and R_2, constitute the biasing network to make sure these is always a $V_{BE} \approx 0.7V$ across both transistors. That way one BJT is always on, and the cross-over region is eliminated.

3.2.3 Preamplifier Stage

The preamp is usually the voltage amplifier part of the audio amp. Since the maximum output voltage from the CD player is about 0.5V, we will require our preamp to have a maximum voltage gain of approximately 20 for all frequencies over the audio range. The Common Emitter amps from Lab 2 are probably not good choices for achieving this gain because they are capacitively or AC coupled, and thus amplify lower frequencies less than higher frequencies in the audio range. (Typically sized coupling capacitors block signals at low range audio frequencies.)

From Lab 1, we know that such a gain is attainable using an op-amp circuit for two main reasons:

(1) Op-amp circuits can be DC coupled thereby allowing us to amplify low frequency signals as well as high frequency signals.

(2) Op-amp circuits are connected with feedback that ensures a flat frequency response over the audio range. Also the use of feedback also reduces distortion.

The preamp stage is also where you would probably want to include volume and tone controls. Volume control can be achieved either by varying the gain of the preamp stage, or by following the preamp with an adjustable voltage divider which will attenuate the signal before it reaches the power stage. 741 op-amps are a reasonable choice for designing the preamp.

3.2.4 Power Amplifier Stage

The power stage of an amplifier usually has unity gain, and supplies current to the load. By looking at the power requirements, we can determine the amount of current which the power stage must source with minimal sagging of the signal. Above we said that the maximum voltage at the load would be about 10V. Thus, the maximum current would be 1.2A. We must now ask ourselves the question, by how much do we have to amplify the output current of the pre-amp, in order to be able to supply 1.2A. In other words, if we consider the input of the power stage to be the load of the preamp stage, what is the load that the preamp stage will drive before significant sagging occurs? The manufacturer's specification sheet says that a 741op-amp has a maximum output current of 20mA. Thus, as designers we probably don't want the 741 to have to source more than about 10mA. Since the 741 will amplify the signal to a maximum amplitude of 10V, then $\frac{10}{0.010} = 1K$ will be the smallest resistance we would want the op-amp to drive. Thus, the input resistance to the transistors of the power stage must be at least 1K to avoid sagging the preamp.

From the preceding discussion we conclude that our power output stage has to be able to source 1.2A and have a minimum input resistance of approximately 1K and unity gain. To achieve this, we could use an ordinary capacitively coupled emitter follower. However, we would like to avoid this because the DC bias requires too much power for efficient operation of power amps. In addition, the AC coupling would cut down on the low frequency response. Probably the best choice for the power stage would thus be a Darlington connected push-pull circuit which is biased slightly on to avoid distortion.

3.2.5 Example Design

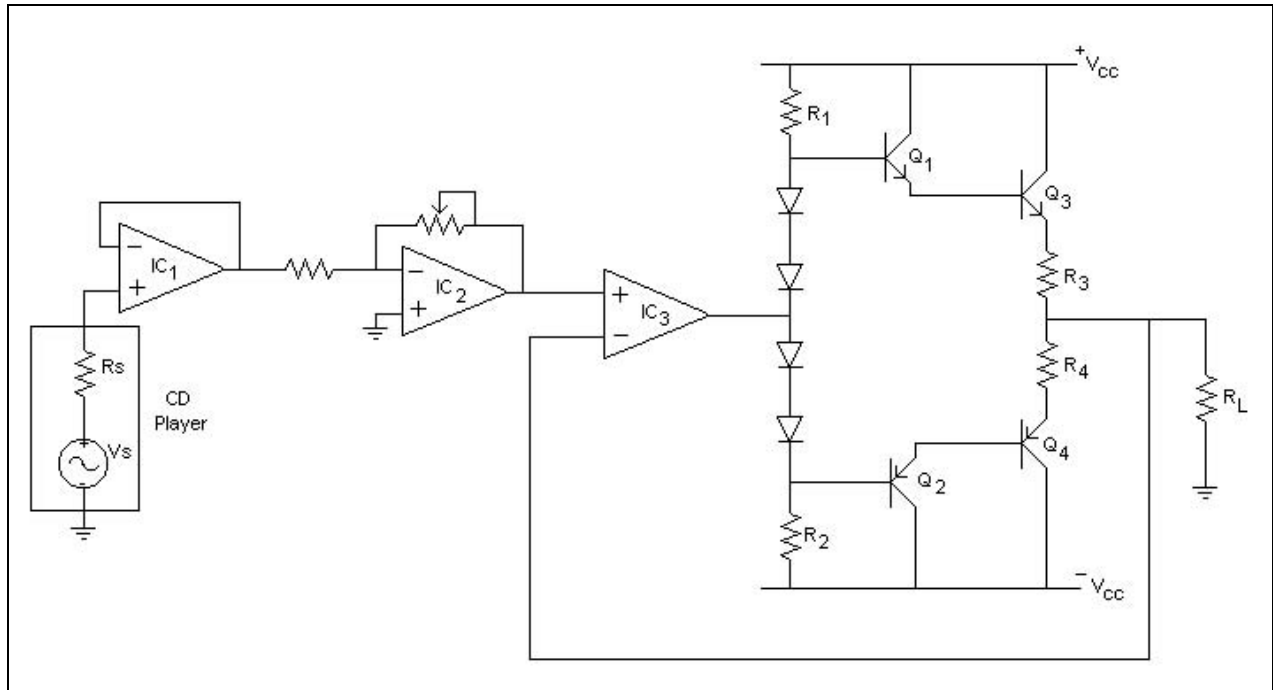An example design of the circuit is given in Fig.3.3.

Figure 3.3: Example Design of Audio Amplifier

IC1 and IC2 are 741's which form the preamplifier stage. IC3 which is also a 741, along with Q1, Q2, Q3 and Q4 form the power stage.

IC1 is an op-amp configured as a voltage follower that isolates the CD player from the rest of the circuit. IC2 is an inverting amp which provides the voltage gain for the circuit. The potentiometer makes the voltage gain variable, thereby giving rise to volume control.

Q1, Q2, Q3 and Q4 form a complementary symmetry (push-pull) Darlington connection output power stage. The Darlington is just another name for connecting two BJT in series as shown to increase the effective current gain to $\beta_1\beta_3$. Q1 and Q3 are npn which are on during positive voltage swings and off during negative swings. Q2 and Q4 are pnp which are off during positive swings and on during negative swings. It is important to determine the power dissipated in the transistors in order to decide what type of transistors to use. D1, D2, D3 and D4 are diodes which act to bias the push-pull output so that it is on the edge of being on with zero input signal, thereby reducing cross-over distortion. R_1 and R_2 isolate the op-amp output from the power supply. R_3 and R_4 act to inhibit thermal runaway by reducing the value of V_{BE} when the junction current (and thus junction temperature) increases. We could have connected the push-pull circuit directly to IC2, however, to reduce distortion an flatten frequency response, we included IC3 along with the feedback connection. The overall effect is then to have a voltage follower with the characteristics of an op-amp, but with its current drive capabilities increased by the addition of Q1 through Q4.

3.3 Experiment: Building the Hi-Fi System

3.3.1 Basic Audio Amp

Design and bread-board an audio frequency amplifier with the ability to supply at least 6 watts to an 8ohm load. To power the amp you will first use the supplies in the lab with rails at $\pm 15V$. Design your amp to have a volume control. The input to your amp will be a CD player. The load will be the bookshelf audio speakers that will be provided in the lab. You want the response to be flat over the entire frequency range. The use of feedback will help achieve a flat frequency response. The amp will be tested and judged according to how good your design is. The only active devices you can use are transistors and op-amps. You can use power transistors which will be made available in the lab. You'll be amazed how good your hi-fi can sound!

1. Begin with the preamp. Use two op-amps like in the pre-amp stage of Fig. (3.3). Set up the first op-amp as a unity gain follower which will isolate the finite output impedance of the CD player from the audio amp. Set up the second op-amp as a voltage amp, with variable gain ranging from 0 to 20. Use a potentiometer in the feedback loop to control the gain, and standard op-amp range resistor values.

2. Measure the preamp input and output voltages. Is the desired gain achieved without distortion?

3. Connect the preamp output directly to the speaker. What happens to the maximum wave form? What is the maximum power that the pre-amp can provide. How loud can it get? (NOTE THAT THE 741 CAN SOURCE ONLY 20mA. If MORE THAN 20mA ARE ATTEMPTED TO BE DRAWN FROM THE 741, CIRCUIT PROTECTION AUTOMATICALLY GETS TURNED ON TO KEEP THE OP-AMP FROM BURNING UP. MOST CIRCUITS DO NOT HAVE SUCH NICE FEATURES, SO CIRCUIT DAMAGE CAN OFTEN OCCUR WHEN SHORTING OUTPUT TO GROUND OR LOW IMPEDANCES.)

4. Breadboard the power stage independently. Use the 2N3904 and 2N3906 BJT's for Q1 and Q2 respectively. For Q3 and Q4 use the power transistors supplied by your lab instructor. For R_1 and R_2 use 5K resistors, and for R_3 and R_4 use 1Ω resistors. For R_L use a 10K resistor. Connect the negative feedback as shown, and for now, ground the input to IC3. The following questions refer to the power stage.

   - What is the voltage gain of the circuit? Recall, the large open loop gain of the op-amp combined with feedback will cause the output to adjust itself so $V^+ = V^-$.

   - What is the current gain of the circuit. From the manufacturer's specification sheet, you will see that the β of the 3904/3906 is approximately 200, while that of the power transistor is 100.

- Check the DC bias conditions. Does $V_o = 0$ for $V_{in} = 0$? Are the DC voltage levels symmetrically distributed around zero volts? Are all the transistors in forward active, and the diodes appropriately on?

- Apply a signal from your function generator directly to IC3. Does the measured voltage gain agree with your predicted value?

5. Connect the two stages together while still using only the 10K load. Apply a 1kHz 0.5V signal from the function generator to the circuit. Observe the output while varying the gain of your amplifier. Vary the input frequency between 100Hz and 15kHz. Make sure your amp is performing to your satisfaction.

6. Connect the CD player to the input of your circuit. Compare the output and input signals. Vary your voltage gain. Is the output an enlarged replica of the input? What is the maximum output voltage before clipping occurs?

7. After you are satisfied with the performance of your amp with the 10K load, turn down the volume and power and connect the speaker to the output. Gradually turn up the power and then the volume. Observe and listen to your signal. Comment on its quality.

8. Replace the lab power supply with one similar to the one your made in Lab 1. Now your amp is totally built by you! How does it work? Congratulations!

9. Measure the frequency response of your amp. Turn the volume to a moderate level. Use the signal generator as your input and sweep it over the audio range. Is the gain constant for all frequencies?

10. What is the maximum power conversion efficiency of your circuit? Does your theoretical value agree with your measured value?

3.3.2 Tone Controls

Extra Credit Design and implement a tone control circuit that will increase or decrease the level of the base or treble of the circuit. This is usually accomplished with an active variable filter type circuit after IC2.

3.4 Preliminary Questions

1. Describe qualitatively the operation of the circuit in Fig. 3.1.

2. For the circuit in Fig. 3.1, take $R_S = 1K$, $R_L = 1K$, the supply voltages to be $\pm 15V$, and V_s to have an amplitude of 10V. Calculate g_m based on the average current. Calculate the voltage gain and output resistance of the circuit.

3. Describe qualitatively the operation of the circuit in Fig. 3.3. What is the purpose of R_1, R_2 and the diodes? What is the purpose of the Darlington connections?

4. If the feedback and input resistors of IC2 are 10K and 1K respectively, what is the voltage gain of the circuit in Fig. 3.3?

5. What is the output resistance of the circuit?

6. What is the current gain?

Laboratory 4

Frequency Response of Simple Transistor Circuits

4.1 Introduction

In Lab 2 we only considered midband frequencies, which were high enough so that coupling capacitors could be treated as short circuits for AC, and low enough that the intrinsic capacitances of the transistor could be ignored. In this lab, we will remove this constraint and examine how frequency affects circuit performance.

In general, the frequency-dependent gain $A(s)$ of amplifier circuits can usually be expressed as

$$A(s) = A_M F_L(s) F_H(s) \qquad (4.1)$$

Where $s = j\omega$ is the complex frequency, A_M is the midband gain, $F_L(s)$ describes the low frequency response, and $F_H(s)$ describes the high frequency response. Ironically, F_L usually represents a high pass filter, and F_H usually represents a low pass filter. The general frequency response usually has the overall characteristics shown in Fig.4.1.

In this lab, you will investigate how this response comes about. First, we will first examine the brute force direct approach for low frequency signals, then we will discuss the Miller effect, as well as single pole approximation approaches. For all experiments use general purpose BJT's such as the 2N3904.

4.2 Low Frequency Brute Force Approach

Consider the CE amp circuit in Fig.4.2. To analyze this circuit, we can divide it into the three sections. It is also useful to replace stage 2 with its amplifier equivalent circuit as shown in lab 2. The small signal equivalent circuit diagram which results is shown in Fig. 4.3.

Since R_{in}, A, and R_{out} are already known from the Lab 2, finding the gain just becomes a simple exercise in analyzing a two voltage dividers. More specifically, we can write the
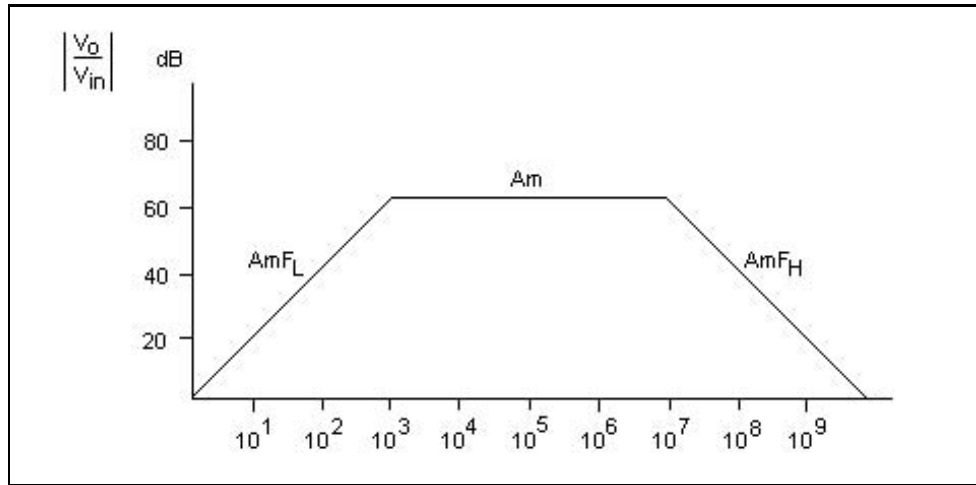
Figure 4.1: Typical Amplifier Frequency Response

voltage gain as the product of the gains of each of the three stages. So, the overall gain is $\frac{v_{out}}{v_{in}} = \frac{v_1}{v_{in}} \frac{Av_1}{v_1} \frac{v_{out}}{Av_1}$. We now take each stage individually. The voltage divider, which is the first stage, gives:

$$\frac{v_1}{v_{in}} = \frac{R_{in}}{R_{in} + \frac{1}{sC_1}} \tag{4.2}$$

Recall from Lab 2 that the gain A of CE amp is

$$A = \frac{-R_C}{R_E + \frac{1}{g_m}} \tag{4.3}$$

The gain of the third stage is also a voltage divider which gives

$$\frac{v_o}{Av_1} = \frac{R_L}{R_L + R_C + \frac{1}{sC_2}} \tag{4.4}$$

The total gain is thus the product of the individual gains of the three stages:

$$\frac{v_{out}}{v_{in}} = \left(\frac{R_{in}}{R_{in} + \frac{1}{sC_1}} \right) \left(\frac{-R_C}{R_E + \frac{1}{g_m}} \right) \left(\frac{R_L}{R_L + R_C + \frac{1}{sC_2}} \right) \tag{4.5}$$

Where, we found from Lab 2 that $R_{in} = R_B || (r_\pi + \beta R_E)$, and $R_o = R_C$.

Poles, Zeros and the Transfer Function

To understand the effects of the capacitors, it is often useful to re-arrange equation (4.5) in the following form:

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_C || R_L}{R_E + \frac{1}{g_m}} \right) \left(\frac{s - 0}{s + \frac{1}{R_{in}C_1}} \right) \left(\frac{s - 0}{s + \frac{1}{C_2(R_L + R_C)}} \right) \tag{4.6}$$
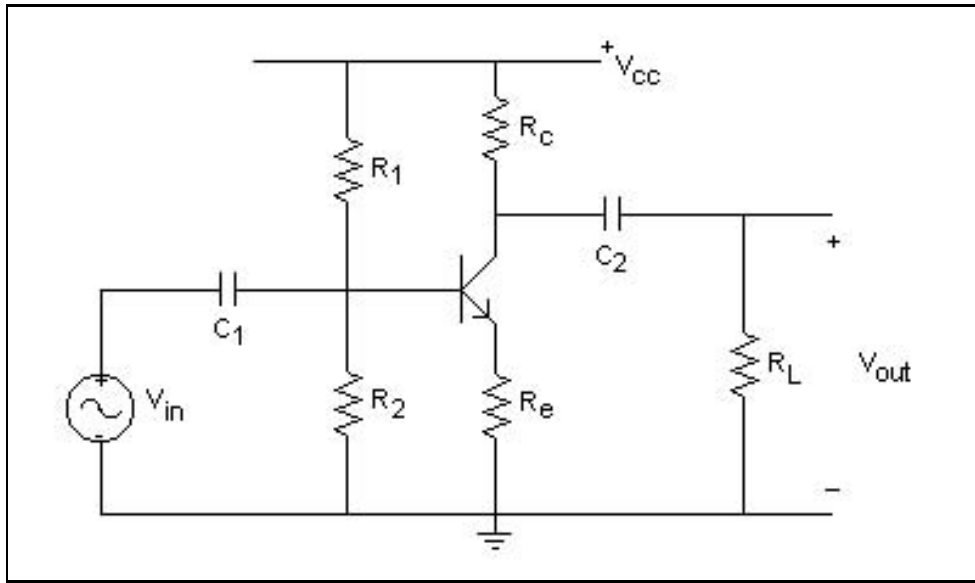
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Figure 4.2: AC Coupled Common Emitter Amp.

The first term in the parentheses of equation (4.6) represents the midband gain, the second term represents the high pass filter at the input, and the third term comes from the high pass filter at the output.

In electronics, it is useful to write polynomial expressions like those in equation (4.6) in the notation of what is commonly known as poles and zeros. If we define zeros as $z_1 = 0$ and $z_2 = 0$, and poles as $p_1 = \frac{-1}{R_{in}C_1}$ and $p_2 = \frac{-1}{C_2(R_L+R_o)}$, then equation (4.7) can again be expressed as:

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_C||R_L}{R_E + \frac{1}{g_m}}\right)\left(\frac{s-z_1}{s-p_1}\right)\left(\frac{s-z_2}{s-p_2}\right) \tag{4.7}$$

As can be seen from equation (4.7), the zeros are the constants in each factor of the form
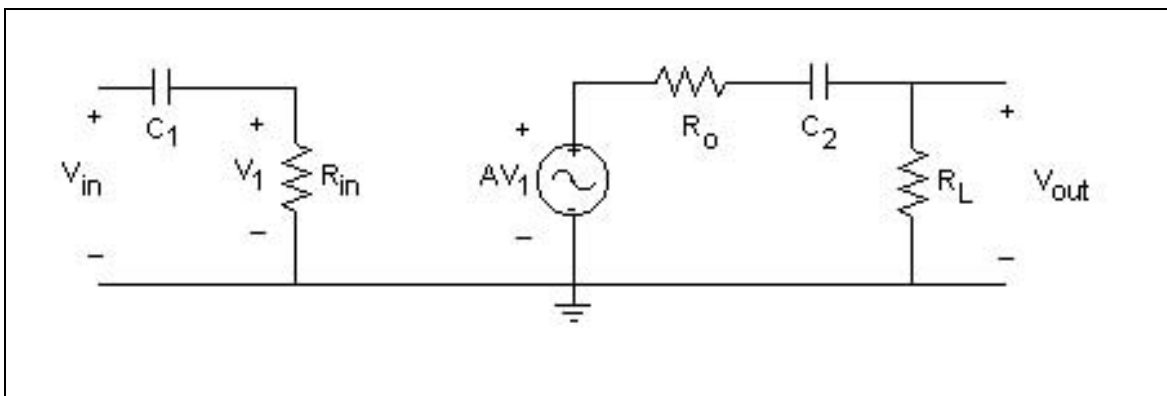

Figure 4.3: AC Coupled Amp with Equivalent Voltage Amp Circuit

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$(s-z)$ found in the numerator of the equation. The poles, on the other hand, are the constants in each factor of the form $(s - p)$ found in the denominator. The overall equation for $\frac{v_{out}}{v_{in}}$ is called the transfer function. The poles and zeros are important because they indicate the angular frequencies where changes in the transfer function occur. In the notation of poles and zeros, we describe equation (4.7) as a second order transfer function with zeros $z_1 = 0$, $z_2 = 0$, and poles $p_1 = \frac{-1}{R_{in}C_1}$, $p_2 = \frac{-1}{C_2(R_L+R_o)}$.

Bode Plots

The zero and pole notation is especially useful for making approximate graphs of the transfer function which are called Bode plots. A Bode plot is a piecewise straight line approximation of the frequency dependence of the transfer function on a log-log scale. It provides an excellent and simple illustration of the frequency response of a circuit. To make a Bode plot of the magnitude versus frequency of the transfer function, on the horizontal axis, we write the log of the angular frequency ω. (Recall $s = j\omega$.) On the vertical axis we write dB, which is defined as $20log\left|\frac{v_o(s)}{v_{in}(s)}\right|$. In other words, if $\left|\frac{v_o(s)}{v_{in}(s)}\right| = 100$, then we say the gain is $40dB$, and if $\left|\frac{v_o(s)}{v_{in}(s)}\right| = 1000$. then we say the gain is $60dB$, etc. Using these axes, the Bode plot is then constructed as an approximate, log-log plot of the transfer function using straight lines in the following way: Starting at low frequencies, and moving toward higher ones, for each zero, we change the slope of the transfer function by $+20$dB/decade, where a decade is a power of 10 change in frequency. For each pole, we change the slope of the transfer function by -20dB/decade (recall $s = j\omega$).

Let's first illustrate this with a relatively arbitrary example by constructing a Bode plot of the transfer function in equation 4.8 with $\frac{v_{out}}{v_{in}}$ given by

$$\frac{v_{out}}{v_{in}} = \frac{10^6(s + 10)(s + 10^2)}{(s + 10^3)(s + 10^4)(s + 10^6)} \tag{4.8}$$

So the above expression has zeros of $z_1 = -10$ and $z_2 = -10^2$, and has poles of $p_1 = -10^3$, $p_2 = -10^4$, and $p_3 = -10^6$. Next, let's factor the poles and zeros out from each term:

$$\frac{v_{out}}{v_{in}} = \frac{10^6 * 10 * 10^2}{10^3 * 10^4 * 10^6} \frac{(\frac{s}{10} + 1)(\frac{s}{10^2} + 1)}{(\frac{s}{10^3} + 1)(\frac{s}{10^4} + 1)(\frac{s}{10^6} + 1)} \tag{4.9}$$

To obtain a Bode plot we now start by taking the $20log$ of the coefficient which is $20log\left(\frac{10^6*10*10^2}{10^3*10^4*10^6}\right) = -80$ We now start plotting at frequency one decade less than the minimum pole or zero, beginning by starting to draw a horizontal line at -80dB from $\omega = 1rad/sec$ to $10rad/sec$. At $\omega = 10rad/sec$, we encounter a zero, so we increase the slope to 20dB/dec. We continue drawing a straight line with this slope until we reach $\omega = 100rad/sec$, where we encounter another zero, and thus increase the slope another 20dB/dec to a total slope of 40dB/dec. We now continue along this slope until we reach the first pole which is at $\omega = 10^3rad/sec$ where we decrease the slope by 20dB/dec to 20dB/dec. We now continue at this slope until we reach the second pole where decrease the slope another 20dB/dec to

0dB/dec. We then continue to draw this horizontal line until we reach the final pole which will give a drop of 20dB/dec. The resulting Bode plot, which is shown in Fig. 4.4.
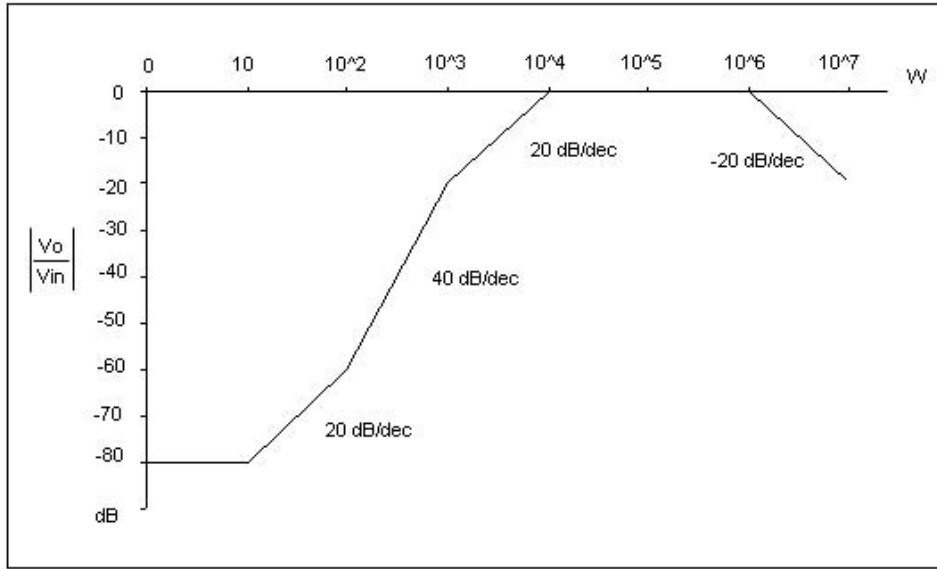

Figure 4.4: Bode Plot Illustration of Equation (4.9)

It is important to notice that the largest value the Bode plot obtained was 0dB. This not an accident. It results because the original expression given by equation (4.8) was characteristic of passive circuits, which are circuits that do not have active gain elements such as transistors or op-amps.

Now, let's obtain a Bode plot for our original circuit of Fig. 4.2. The equation describing frequency-dependent gain of that circuit is given by equation 4.6. Let's factor out the poles to obtain a form similar to that of equation (4.9).

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_C || R_L}{R_E + \frac{1}{g_m}} \right) \left[\frac{s^2 R_{in} C_1 (R_L + R_C) C_2}{(s R_{in} C_1 + 1)(s C_2 (R_L + R_C) + 1)} \right] \tag{4.10}$$

First let's plot the frequency-dependent fractional part, and then add the constant coefficients. Starting with the numerator, we have 2 zeros at $\omega = 0$, this gives rise to a line with slope of 40dB/dec which is zero dB at $\omega = 1$. At $\omega = |p_1|$ the slope changes to 20dB/dec, and finally at $\omega = |p_2|$ the slope decreases by another 20dB/dec to become a horizontal line. Now we add $20log(R_{in}C_1)(C_2(R_L + R_C))$. to obtain the response of the passive part of the transfer function only. Finally, we add the midband gain $20log\frac{R_C||R_L}{1/g_m + R_E}$ to obtain a graph of the entire equation.

We have just illustrated in detail the mechanics of drawing a Bode plot. However, they can usually be drawn very quickly for the midband to low frequency part of a response with the following approach. Start by finding the highest frequency low-frequency pole, and draw a horizontal line at that point for the midband gain. Next, move to the left (direction of

decreasing ω), and for each pole you encounter increase your slope downward by 20dB/dec, and for each zero you encounter decrease your downward slope by 20dB/dec. In a sense, it is a very quick method of obtaining the same result we described in detail above. The resulting Bode plot is sketched in Fig. 4.5.
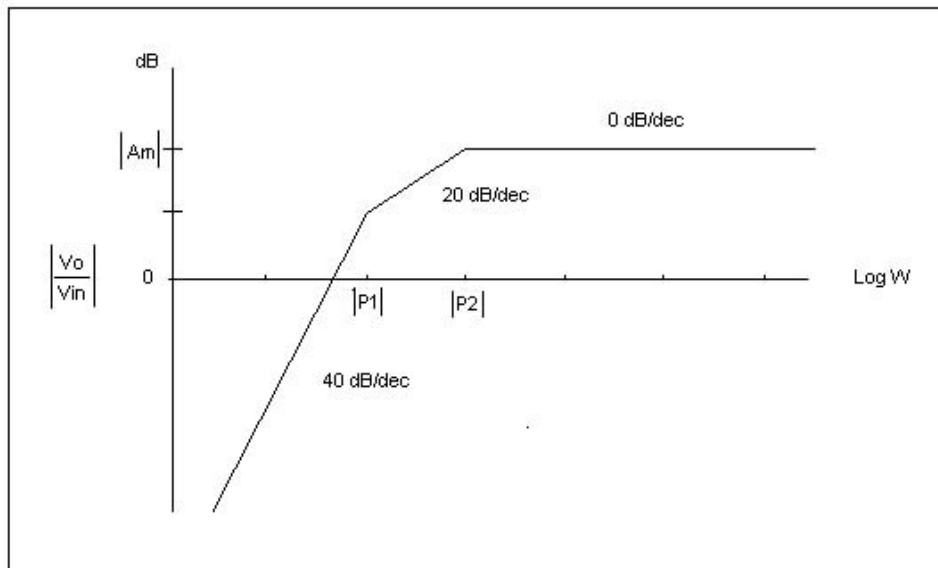

Figure 4.5: Bode Plot Illustration of Equation (4.10)

4.3   CE Amp with Emitter Bypass Capacitor

In electronics, it is often useful to bypass the emitter resistor with a capacitor as shown in Fig. 4.6. This configuration is useful since at midband frequencies, C_E acts to short the resistor R_E, thereby increasing the gain. But at DC, the presence of R_E facilitates achieving the desired DC bias point. The gain of the circuit in Fig. 4.6 is thus very similar to that in Fig. 4.3, except R_E is replaced with $Z_E = R_E||\frac{1}{sC_E}$, and R_{in} is replaced with $Z_{in} = R_B||(r_\pi + \beta Z_E)$. Thus, the expression for voltage gain of the emiter-bypassed CE amp is

$$\frac{v_{out}}{v_{in}} = \left(\frac{Z_{in}}{Z_{in} + \frac{1}{sC_1}}\right)\left(\frac{-R_C}{Z_E + \frac{1}{g_m}}\right)\left(\frac{R_L}{R_L + R_C + \frac{1}{sC_2}}\right) \tag{4.11}$$

If the frequency increases towards the midband limit, then the impedances of the capacitors goes to zero and the expression for gain becomes

$$\frac{v_{out}}{v_{in}} \approx \frac{-g_m R_C R_L}{R_L + R_C} = -g_m(R_C||R_L) \tag{4.12}$$

While the preceding expression is fairly simple, if we want to get a specific expression for the frequency-dependent gain of the CE amp in Fig.4.6, we have to put in explicit forms given
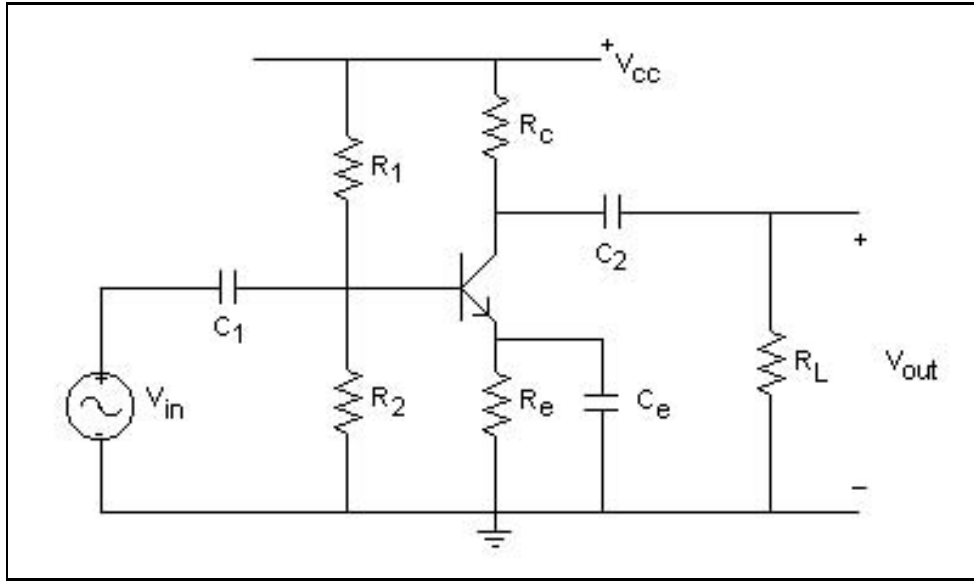
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Figure 4.6: CE Amp with Emitter Bypass Capacitor

above for Z_E and Z_{in}. Upon doing so we obtain the following fairly messy expression:

$$\frac{V_{out}}{V_{in}} = \left(\frac{s^2 R_E r_\pi C_1 C_E + s(r_\pi C_1 + R_E C_1)}{s^2 C_1 C_E R_E r_\pi + s(C_1 r_\pi + C_1 R_E + C_E R_E) + 1}\right)\left(\frac{-g_m R_C(s R_E C_E + 1)}{s R_E C_E + R_E g_m + 1}\right)\left(\frac{R_L}{R_L + R_C + \frac{1}{sC_2}}\right)$$
(4.13)

It's interesting to note that when s becomes very large (4.13) reduces to (4.12), which is the expected result.

4.4   Short Circuit Time-Constant Approximation (SCTCA)

Equation (4.13) is accurate, but it's not clear that it is very useful. We could program it and evaluate it numerically. That would give us the behavior. Another, probably more useful approach would be to find the roots of all the polynomials on the numerator and denominator. That would give all the poles and zeros. Then a Bode plot could be performed to give the response of the circuit. However, this would still require more algebra than you may want to do. Another way is to realize that all the filters in the circuit are of the high-pass type, and tend to yield increasing gain with frequency. It's also worth noticing that there are the same number of poles as there are zeros. Under these circumstances, it's expedient to use the *Short-Circuit Time Constant Approximation* (SCTCA).

With the SCTCA we approximate the combined effect of all the poles and zeros to make a single first order high pass filter. In other words, we approximate the gain of the overall circuit as

$$\frac{V_{out}}{V_{in}} = A_m \frac{s}{s - p_o}$$
(4.14)

Where A_m is the midband voltage gain, and p_o is the single pole that approximates the combined effects of the actual poles and zeros of the circuit. To determine p_o, you determine the resistance seen by each capacitor, while all the other capacitors are shorted. We then multiply the resistance seen by the value of the capacitor of interest to obtain the short-circuit time constant for that capacitor. This procedure is then repeated for all capacitors which govern the low frequency response. Finally, p_o is then given by the sum of the reciprocal of each time constant. Mathematically, this is expressed as:

$$p_o \approx \sum_i \frac{-1}{R_i C_i} \qquad (4.15)$$

Where R_i is the resistance seen by the $i'th$ capacitor with all other capacitors shorted.

4.5 Experiment: Low Frequency Response of CE Amp

1. Using techniques for Lab 2, design a CE amp circuit with midband gain of 15. Bias the circuit so that the swing is approximately maximum. For coupling capacitors use $C_1 = C_2 = 0.1\mu F$ Do NOT use an emitter bypass capacitor. (If you used typical values for R_1, R_2, R_C and R_E, then you should reach the midband region at approximately $\omega \approx 10KHz$.)

2. Measure the gain of the circuit at midband and determine if your design agree with experiment.

3. Use the SCTCA to approximate the frequency response of the circuit.

4. Measure the gain as a function of frequency and determine the error of the SCTCA. Start at 10Hz and increase your frequency to 100kHz, making about two measurements per decade.

5. Sketch a Bode plot of the theoretical and experimental responses of the circuits.

6. Add a $0.1\mu F$ bypass emitter capacitor in parallel with the emitter resistor. Use the SCTCA to approximate the frequency response of the circuit. Measure the gain as a function of frequency and compare to your calculations. Start at 10Hz and increase your frequency to 100kHz, making about two measurements per decade.

7. Sketch a Bode plot of the theoretical and experimental responses of the circuits.

4.6 High Frequency Response Using Miller's Approximation

At high frequencies, the voltage gain of amplifiers usually decreases. To demonstrate this consider the circuit in Fig.4.7.
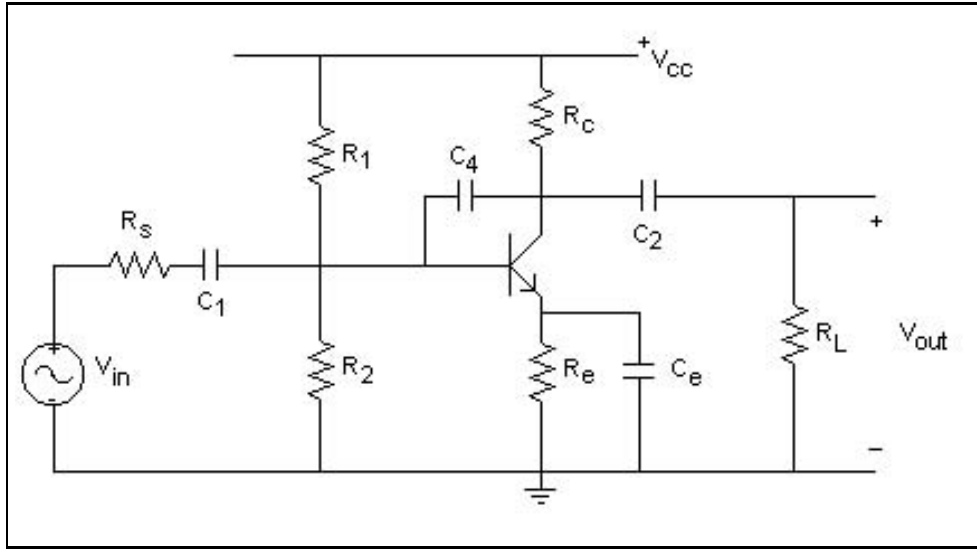
Figure 4.7: CE Amp with Miller Capacitor

As we saw in the preceding sections, capacitors C_1, C_2 and C_E tend to give rise to increasing gain with high frequency. Here, on the other hand, we have another capacitor C_4, which tends to cause the gain to decrease as frequency increases. The effect of this capacitor can be explained qualitatively by the following discussion. Recall that the signal at the collector is approximately 180° out of phase with the input signal at the base. The capacitor C_4 provides a path for some of that signal at the collector to be fed back to the base. Since collector signal is out of phase with the base signal, this feedback has the effect of partially canceling the input signal at the base. Since the total signal going into the base is thus reduced, the overall gain decreases. It can be shown that the effect of the capacitor C_4 can be approximated by the circuit in Fig. 4.8, which is known as *Miller's Approximation*.

The circuit shows that the effect of C_4 can be modeled by replacing it by C_M to ground, where C_M is given by

$$C_M = (|A| + 1)C_4 \tag{4.16}$$

Where A_m is the midband gain of the amplifier stage. For example, if the circuit in Fig. 4.7 has a midband gain of $-g_m R_C || R_L$, then $C_M = (g_m R_C || R_L + 1)C_4$. As implied by Fig. 4.8, the base signal then sees a low pass filter consisting of R_S, C_M and R_{in}, thereby attenuating the high frequency response of the circuits. For example, the gain of the amplifier in Fig. 4.7, assuming that the frequency is high enough so that C_1, C_2, C_E can be considered short circuits, is given by

$$\frac{v_{out}}{v_s} = \frac{-R_{in}||\frac{1}{sC_M}}{R_{in}||\frac{1}{sC_M} + R_S} g_m R_C || R_L \tag{4.17}$$
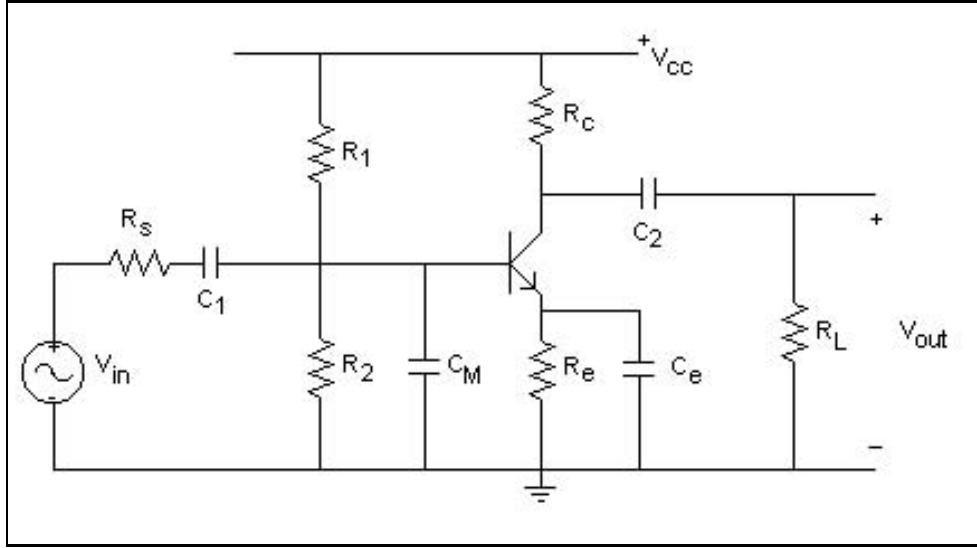
Figure 4.8: CF Amp using Miller's Approximation

It is interesting to note that Equation (4.17) can be arranged into the following:

$$\frac{v_{out}}{v_s} = \left(\frac{-R_{in}}{R_{in} + R_S} g_m R_C || R_L \right) \left(\frac{1}{1 + \frac{sC_M R_{in} R_S}{R_{in} + R_S}} \right) \tag{4.18}$$

By recalling the results from Chp. 2, we can see that the expression in the first set of parentheses is the midband gain A_m. Furthermore, the expression in the second parentheses is just that of a first order low pass filter, with the pole $p = -\frac{R_{in} + R_S}{C_M R_{in} R_S}$. Thus, we can express the gain of the circuit at high frequencies as a midband gain A_m multiplied by a low pass filter response.

$$A(s) = A_m \frac{1}{1 - \frac{s}{p}} \tag{4.19}$$

The Bode plot for the high frequency response given by equation (4.18) can quickly be drawn starting with a horizontal line of magnitude $20 log \frac{-R_{in}}{R_{in} + R_S} g_m R_C || R_L$, and then having the gain fall off with a slope of $20 dB/dec$ at frequencies $\omega \geq \frac{R_{in} + R_S}{C_M R_{in} R_S}$

4.6.1 Miller Time Constant Approach

Equation (4.19) tells us that the effect of the Miller capacitor can be easily approximated by finding the midband gain, and the value of the pole p. An easy way to determine the value of p is to notice that

$$p = \frac{-1}{R_M C_M} \tag{4.20}$$

Where R_M is the resistance seen by the Miller capacitor C_M (Note that the emitter capacitor C_E shorts R_E).

$$R_M = R_{in} || R_S = R_B || (r_\pi) || R_S \tag{4.21}$$

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In summary, we've been trying to show that the overall strategy for approximating the effect of the Miller capacitor, is to determine the midband gain, and then multiply that gain by the expression for a first order low pass filter, with pole determined by $\frac{1}{R_M C_M}$.

4.7 Experiment: Miller Effect and High Frequency Response Part I
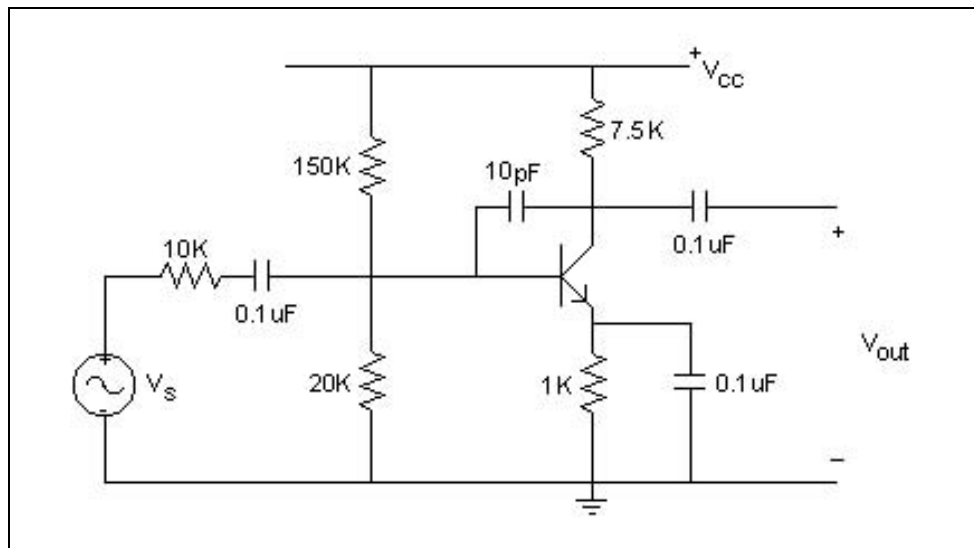

Figure 4.9: Circuit for demonstrating Miller effect

1. Construct the circuit in Fig.4.9, take $V_{CC} = 15V$.

2. Use Miller's approximation to theoretically estimate the high frequency response of your circuit.

3. Use the SCTCA to theoretical estimate the low frequency response of the circuit.

4. Measure the frequency response of the circuit by measuring the gain at every frequency decade starting from 10Hz and ending at 10MHz.

5. On at Bode plot, sketch the gain versus frequency of both the theoretical results and the measured ones.

4.8 Transistor Intrinsic Capacitance

Transistors have internal capacitances that are usually not wanted and act to reduce the gain at high frequencies. In BJT's these intrinsic capacitors come from the construction

of the device itself and are usually associated with its internal PN junctions. In BJT's we usually label C_μ as the capacitance associated with the base-collector junction, and C_π the capacitance associated with the base-emitter junction. These capacitances are illustrated in Fig. 4.10. In the right side of the figure we have drawn the small signal equivalent circuit,
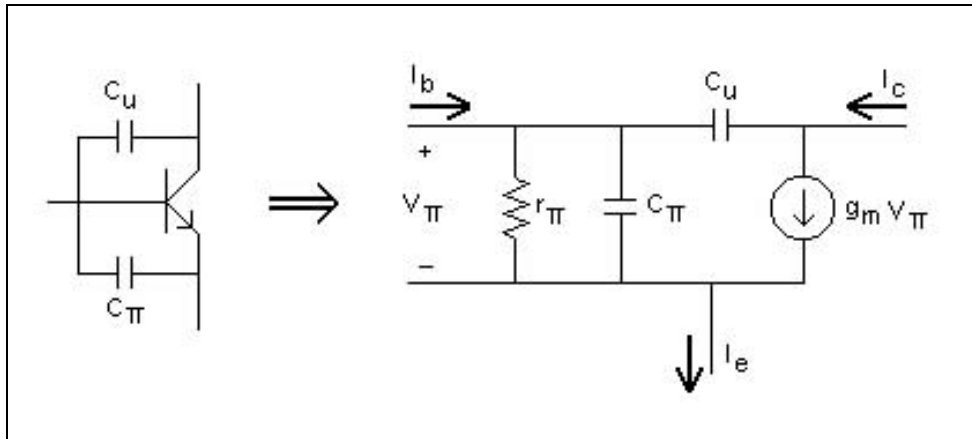

Figure 4.10: Equivalent Circuit Showing BJT Intrinsic Capacitances

which is usually very useful for analyzing the effect of this response.

4.9 High Frequency Response Using Open Circuit Time Constant Analysis(OCTCA)

From the above equivalent circuit, we could use KVL and KCL to rigorously analyze the small signal response. However, once we have more than one transistor in a circuit, such an approach becomes impractical, and designers usually opt for approximate methods. As can be seen, C_μ is actually a Miller capacitance, and we can analyze it as such. However, another approach to analyze these effects is the Open Circuit Time Constant Analysis (OCTCA), which we will introduce here.

Very often a circuit contains a dominant pole which largely determines its high-frequency characteristics. The OCTCA gives a methodology for approximating the value of this dominant pole. With the OCTCA, you account for the effect of one high-frequency capacitor at a time. You do this by determining the resistance seen by C_π, while assuming C_μ is not there (open circuited). You then repeat the process by determining the resistance seen by C_μ, while open circuiting C_π. If there were more high frequency capacitors in the circuit, you would repeat this process for each capacitor. The high frequency response is then approximated by a low pass filter with a single pole

$$p = \frac{-1}{\sum_i R_i C_i} \tag{4.22}$$

Where R_i is the resistance seen by C_i with all other high frequency capacitors open.

The OCTCA approach is probably best illustrated through example. Consider the CE amp in Fig. 4.11 Let's start by drawing the small signal equivalent circuit which is shown in
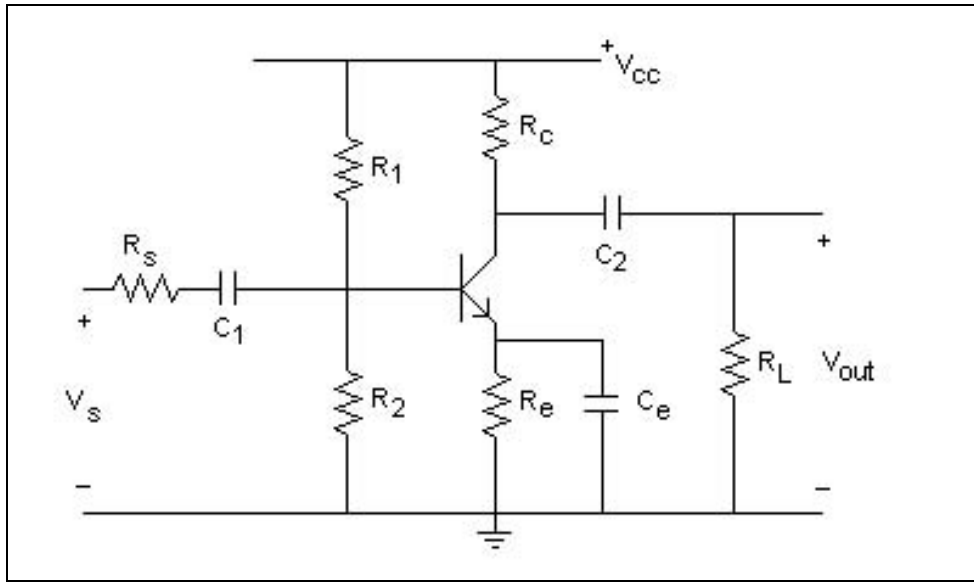

Figure 4.11: Circuit for Illustrating OCTCA

Fig. 4.13. Notice that we have explicitly included the intrinsic capacitors C_π and C_μ. Now, we can divide the capacitors into two groups. The first group tend to give rise to higher voltage gain as the frequency increases. This group consists of C_1, C_2 and C_E. The second group causes the gain to decrease as frequency increases. This group consists of C_π and C_μ. Now, let's consider only frequencies which are so high that C_1, C_2 and C_E can be considered short circuits. Under these circumstances the small signal equivalent circuit is shown in Fig. 4.13 Of course we could now analyze this circuit formally using loop equations to obtain the voltage gain as a function of frequency. However, once circuits contain more than one transistor, such analyses become very tedious, and are usually best done numerically. Here, we illustrate the OCTCA which is easily extendible to complex circuits.

As mentioned above, with the OCTCA we open all capacitors and short the input. Then, we determine resistance seen by the capacitor under consideration. Let's start with C_π. First we open C_μ. The resistance C_π sees with C_μ open is then $R_S||R_B||r_\pi = R_{\pi o}$. So, the contribution due to capacitor C_π can be approximated with the time constant $\tau_\pi = R_{\pi o}C_\pi$.

Determining the resistance seen by C_μ is not quite as obvious due to the dependent current source. To determine this resistance, which we will designate $R_{\mu o}$, we first open C_π, and then replace C_μ with a current source and determine the voltage developed across it. The situation is illustrated in Fig. 4.14. In this figure, i_x is the value of the test current source which replaces C_μ, and $v_1 - v_2$ is the voltage developed across i_x. Also in the figure $R'_L = R_C||R_L$ and v_π is the voltage across $R_{\pi o}$. The resistance seen by C_μ is thus given by

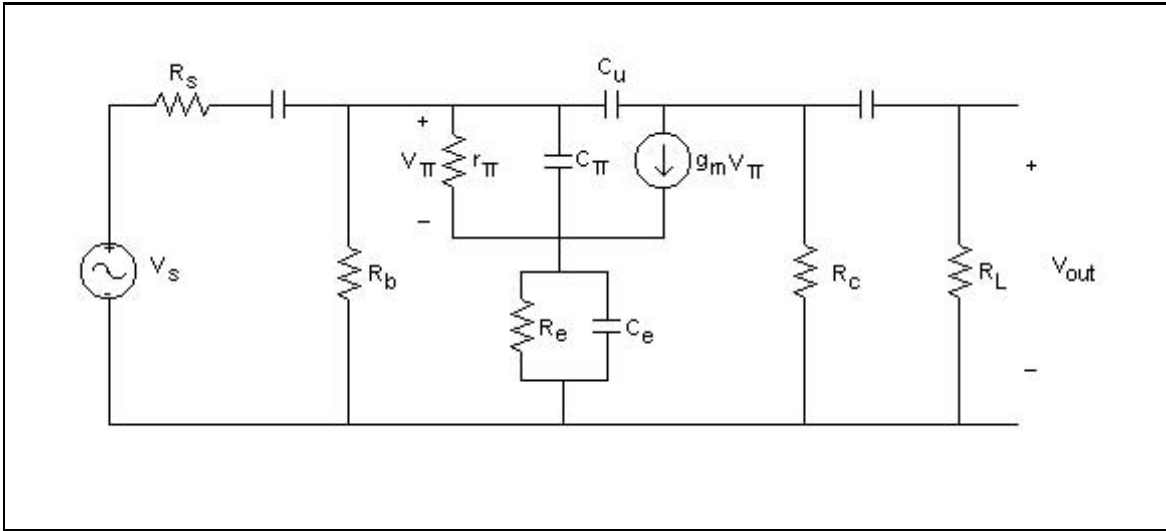$$R_{\mu o} = \frac{v_1 - v_2}{i_x} \tag{4.23}$$

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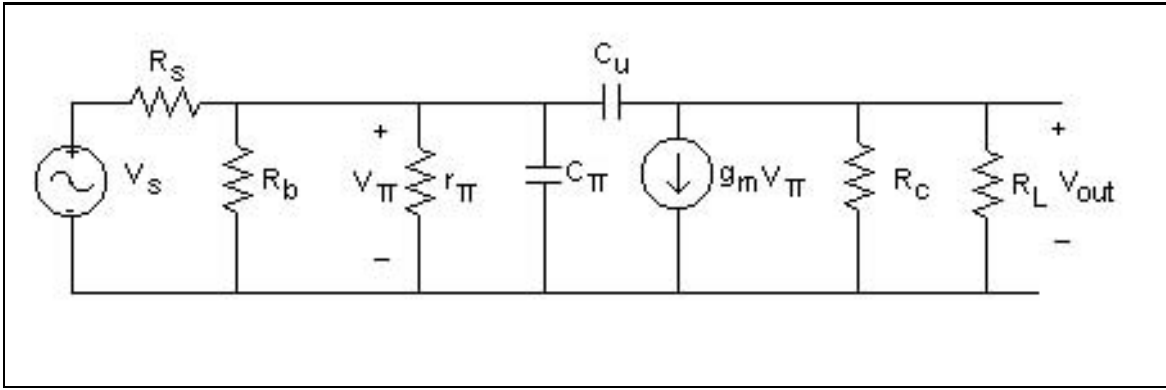Figure 4.12: Small Signal Equivalent Circuit Illustrating OCTCA

Figure 4.13: CE High Frequency Small Signal Equivalent Circuit

To find $R_{\mu o}$ in terms of known quantities apply Kirchoff's laws.

$$v_1 = i_x R_{\pi o} \tag{4.24}$$

$$v_2 = i_x(g_m R_{\pi o} + 1)R'_L \tag{4.25}$$

Therefore, the resistance seen by C_μ is

$$R_{\mu o} = \frac{v_1 - v_2}{i_x} = R_{\pi o} + g_m R_{\pi o} R'_L + R'_L \tag{4.26}$$

Thus, the time constant associated with C_μ is $\tau_\mu = C_\mu R_{\mu o}$.

Using the OCTCA, we approximate the high frequency response of the circuit with a first order low pass filter with a pole p at

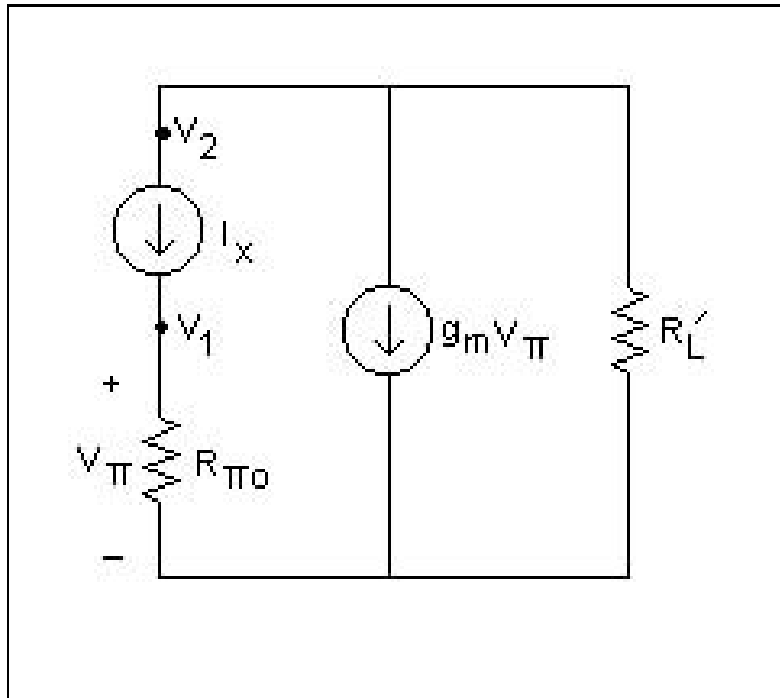$$p = \frac{-1}{\tau_\pi + \tau_\mu} \tag{4.27}$$

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Figure 4.14: Circuit for determining resistance seen by C_μ

The voltage gain $A(s)$ of the circuit at high frequencies is thus approximated by

$$A(s) = \frac{A_m}{1 - \frac{s}{p}} \qquad (4.28)$$

Where A_m is the midband gain.

4.10 Experiment: The OCTCA and High-Frequency Response Due to Intrinsic Capacitances

Use the circuit in Fig. 4.15 to perform this experiment. Set the supply voltage $V_{cc} = 15V$

1. Measure the voltage gain of this circuit as a function of frequency. Take approximately two measurements per/decade, starting from 10Hz and going to 10MHz.

2. Analyze the circuit using the Miller approach, and the OCTCA. From your analysis and your experimental results, provide values for the intrinsic capacitor C_μ. Assume that due to the Miller effect is C_μ is dominant, and C_π can be neglected.

3. **Extra Credit** Now that you have determined C_μ, try to find C_π. To do this, set $R_C = 0$, and measure $\frac{\Delta v_B}{v_{in}}$ and keep in mind that the capacitance that you calculate will be that of C_π and C_μ'' in parallel.
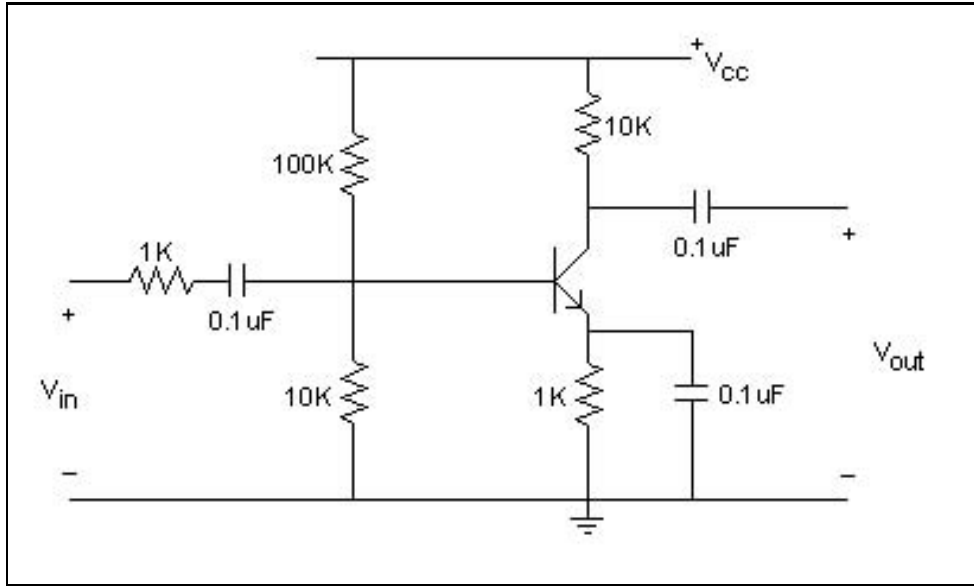
Figure 4.15: Circuit for Measuring High Frequency Intrinsic Capacitors

4.11 Frequency Response of Multi-Transistor Amplifiers

The OCTCA becomes especially useful for multi-transistor circuits where the number of loop equations quickly becomes too numerous for conventional analysis. As an example, consider the typical circuit which contains a CE gain stage followed by an EF buffer stage shown in Fig. 4.16. This circuit has the following high frequency equivalent shown in Fig. 4.17.

Using the OCTCA techniques, we can approximate the dominant pole frequency, and obtain a fairly accurate description of the high-frequency roll-off of the circuit. All we have to do is find the resistance seen by each capacitor individually. The dominant pole is then approximated by

$$p = \frac{-1}{C_{\pi 1}R_{\pi 1} + C_{\mu 1}R_{\mu 1} + C_{\pi 2}R_{\pi 1} + C_{\mu 2}R_{\mu 2}} \tag{4.29}$$

Where

$$R_{\pi 1} = R_S || R_{in1} \tag{4.30}$$

$$R_{\mu 1} = R_{\pi 1} + R_{L1} + g_m R_{L1} R_{\pi 1}, \tag{4.31}$$

$$R_{L1} = R_C || (r_{\pi 2} + \beta R_{E2}) = R_{in2} \tag{4.32}$$

$$R_{\pi 2} = r_{\pi 2} || \frac{R_C + R_{E2}}{1 + g_{m2}R_{E2}} \tag{4.33}$$

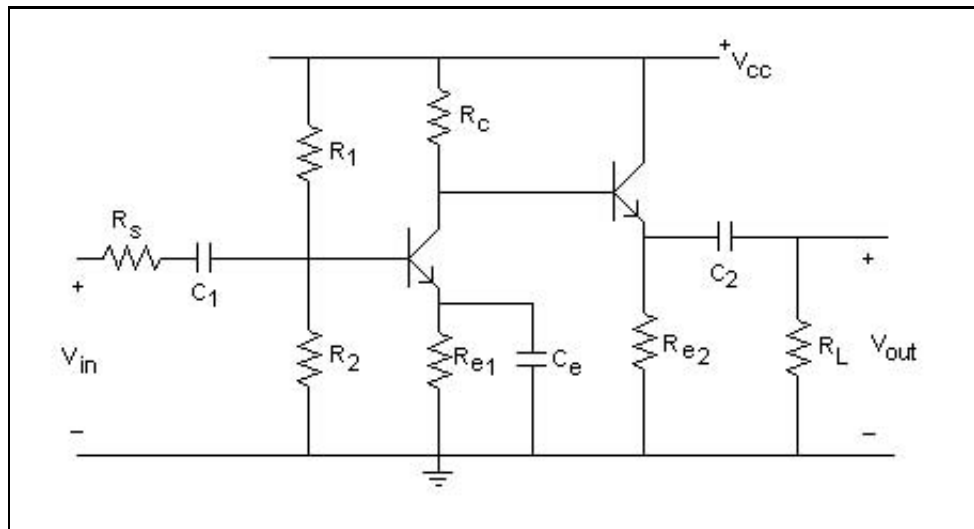$$R_{\mu 2} = R_C || R_{in2} \tag{4.34}$$

Figure 4.16: Typical Two-Transistor Amp

4.12 Experiment: Multi-Transistor Amps.

1. Set up the CE-EF amp shown in Fig. 4.16. Let $R_1 = 100K$, $R_2 = 10K$, $R_C = 10K$, R_{E1}, $R_{E2} = 1K$, $R_L = 10K$, $C_1 = C_2 = C_E = 0.1\mu F$, $V_{CC} = 15V$, and $\beta = 200$.

2. Calculate the midband gain of the circuit.

3. Measure the frequency-dependent gain for each decade ranging from 10Hz to 10MHz.

4. Use the OCTCA to estimate the frequency response of the circuit.

5. Draw a Bode plot of your result of gain versus frequency for the measured and theoretical values.

4.13 Preliminary Questions

1. The following questions refer to Fig. 4.2. Take $R_1 = 90K$, $R_2 = 10K$, $R_C = 7K$, $R_E = 700$, $R_L = \infty$, $C_1 = C_2 = 0.1\mu F$ and $V_{CC} = 15V$.

   - Find the voltage gain at midband frequencies.
   - Use the brute force approach to find the low-band gain versus frequency.
   - Use the SCTCA to approximate the low-band gain versus frequency with a single pole.
   - Sketch your results on a Bode plot.

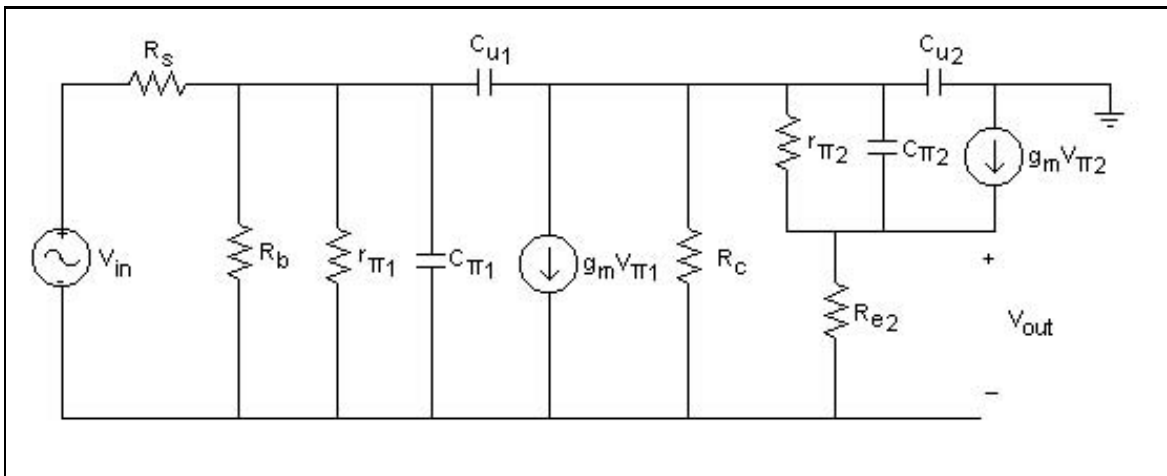2. The following questions refer to the circuit in Fig.4.9.

Figure 4.17: High Frequency Equivalent Circuit of CE-EF Amp

- Calculate the small signal voltage gain at midband frequencies.

- Use the Miller approximation to calculate the dominant high-frequency pole of the circuit.

- Sketch the gain from midband to high frequencies on a Bode plot.

3. The following questions refer to the circuit in Fig.4.15. For this question only, assume that $C_\pi = C_\mu = 1.0pf$ (picofarads).

- Use the SCTCA and the OCTCA to obtain the low and high frequency single pole approximations for the frequency response of this circuit.

- Sketch the gain of this circuit versus frequency from 1Hz to 100MHz on a Bode plot.

Laboratory 5

Differential Amplifiers and Op-Amp Basics

5.1 Introduction

In this lab we build differential amplifiers, which are basic building blocks found throughout electronics. We then combine our differential amplifier circuit, with an emitter follower to form a very simple op-amp-like circuit. Finally, we investigate how we can use feedback to control circuit performance.

5.2 Differential Amplifiers

Differential amplifiers are a fundamental configuration in electronics. Every op-amp has a differential amplifier as its core. Differential amplifiers also form the backbone of many communication circuits such as mixers and modulators. The main characteristics that make differential amplifiers so useful are their large gain, ability to reject noise, and the fact that they amplify the difference between two signals. Below, we first show how one can DC bias a diff-amp, and then demonstrate its AC voltage gain. An example configuration for a differential amplifier is shown in Fig. 5.1. In the figure, Q1 and Q2 form the core of the amplifier, while Q3 acts as a DC current source to bias the circuit. The input can be into the base of either Q1 or Q2, or both, with the small signal output taken either from the collector of Q1, Q2, or both. One important thing to notice is that since the bias is accomplished with Q3, the input signal does not have to be AC coupled through a capacitor like was necessary in the previous transistor voltage amplifier circuits we studied.
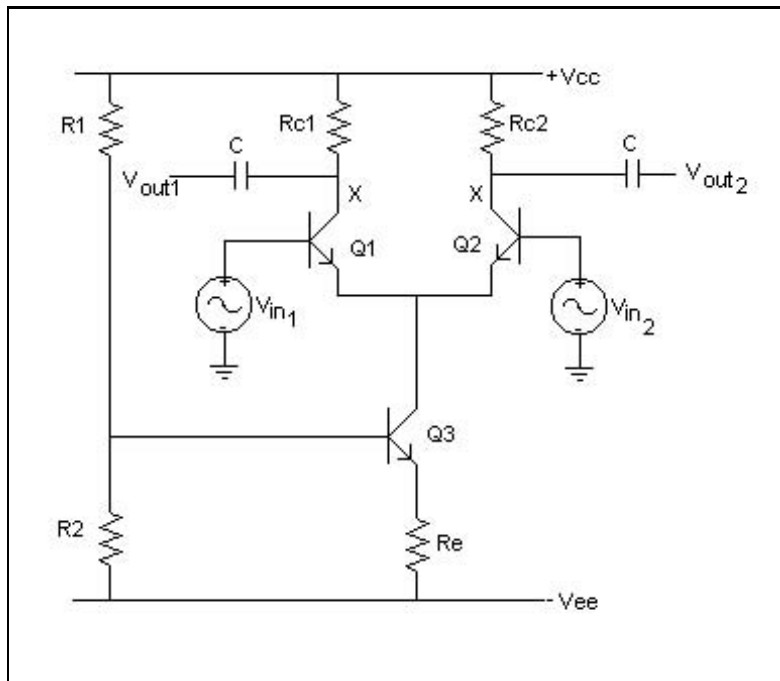
Figure 5.1: Differential Amplifier

5.2.1 Differential Pair DC Bias

The differential amplifier is also called the emitter coupled pair, because, as shown in figure 5.1, it has two transistors Q1 and Q2 with their emitters shorted together.
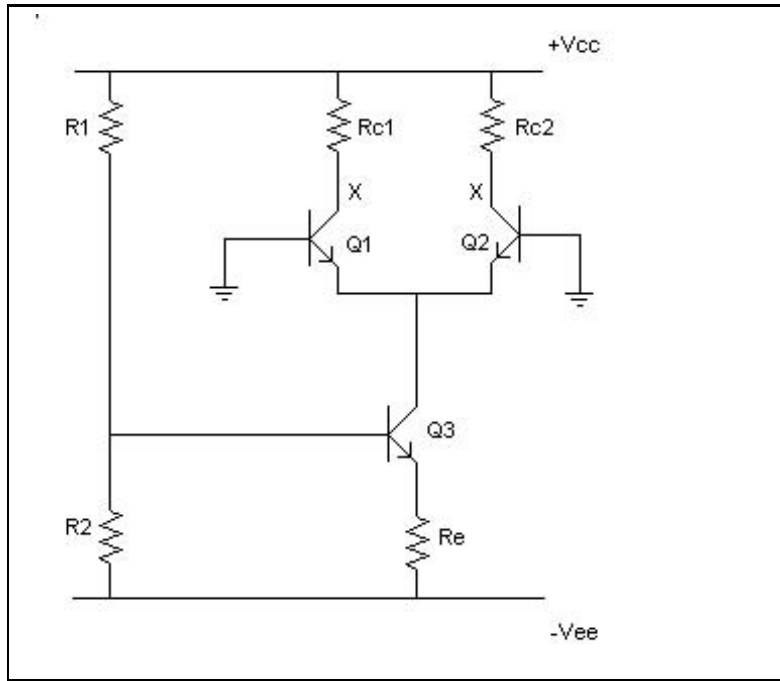
Figure 5.2: Differential Amplifier DC Bias

The emitter coupled pair is biased by a DC current source. In Fig. 5.2, this current source is provided by Q3, which is a common emitter biasing configuration. (In contrast to our previous work, the common emitter configuration of Q3 is not being used as an amplifier, but just to provide a constant current to the emitter coupled pair.) Under ideal conditions, Q3 acts as an ideal DC current source which biases Q1 and Q2. The transistors Q1 and Q2 provide the small signal voltage gain, which we will discuss in the next section. Here, we discuss the DC bias. We first ground the two inputs. Now, we provide DC bias by Q3, and define the DC bias current sunk by collector Q3 as I_{EE}. From KCL it is clear that

$$I_{E1} + I_{E2} = I_{EE} \tag{5.1}$$

Then this bias current is split between Q1 and Q2. so that

$$I_{C1} + I_{C2} = I_{EE} \tag{5.2}$$

Now, let us assume Q1 and Q2 are identical, then the the DC bias current I_{EE} is split evenly between them so

$$I_{E1} = I_{E2} = \frac{I_{EE}}{2} \tag{5.3}$$

We now make the excellent approximation that $I_{E1} = I_{C1} = I_{C2}$. The DC voltage at the collectors of Q1 and Q2 is then

$$V_{C1} = V_{CC} - I_{C1}R_{C1} \tag{5.4}$$

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$$V_{C2} = V_{CC} - I_{C2}R_{C2} \tag{5.5}$$

If $R_{C1} = R_{C2}$, then $V_{C1} = V_{C2}$. Of course, since the bases of Q1 and Q2 are grounded, then

$$V_{E1} = V_{E2} = -V_{BE} \approx -0.7V. \tag{5.6}$$

Just as we did in our other transistor amplifier circuits, for analog operation, we must ensure that Q1 and Q2 are in the forward active region of operation. So, when designing our amplifier, we must make sure that our transistors are not in saturation ($V_C > V_B \approx 0.7$). So, to zero order approximation, we usually choose R_C and I_C so that $V_C \approx \frac{V_{CC}}{2}$. This will help you to obtain virtually maximum swing of your AC signal.

5.2.2   Differential Pair Small Signal Voltage Gain

For the sake of understanding, let's assume we take the small signal output from the collector of Q2, and input the small signal voltage to the base of Q1. This is shown in Fig. 5.3. The
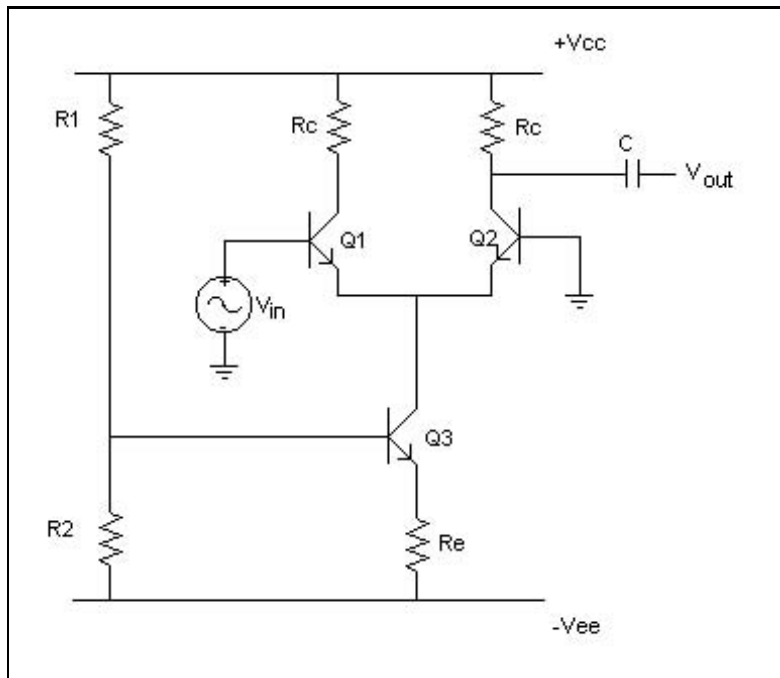

Figure 5.3: Differential Amplifier Single-Ended Differential Mode Gain Configuration

small signal voltage gain will then be defined as the change in the collector voltage at Q2 divided by the change in the base voltage of Q1, or $A_v = \frac{V_o}{V_i} = \frac{\Delta V_{C2}}{\Delta V_{B1}}$. Taking the small signal change of (5.5), we find the small signal output voltage V_o.

$$V_o = \Delta V_c = -\Delta I_{c2}R_C \tag{5.7}$$

To find the small signal change in the input, we start with the large signal KVL equation

$$V_{b1} - V_{b2} = V_{be1} - V_{be2} \tag{5.8}$$

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Now, if we ground V_{b2}, and make a small signal change in V_{b1} we obtain

$$\Delta V_{b1} = \Delta V_{be1} - \Delta V_{be2} \tag{5.9}$$

Recall from previous labs that a first order Taylor series gives $\Delta V_{be} = \frac{\Delta I_c}{g_m}$. We then find that

$$\Delta V_{b1} = \frac{\Delta I_{c1}}{g_{m1}} - \frac{\Delta I_{c2}}{g_{m2}} \tag{5.10}$$

Since $g_m = \frac{I_C}{V_t}$ and, under DC conditions $I_{C1} = I_{C2}$, then

$$g_{m1} = g_{m2} = g_m \tag{5.11}$$

Now, recall that the total current in the diff-amp is determined by the DC bias current I_{EE} which is fixed. Thus, if we make a small increase in I_{c1} then there will be a corresponding small decrease in I_{c2}. We express this mathematically by taking the small signal change of equation (5.2), which gives

$$\Delta I_{c1} + \Delta I_{c2} = \Delta I_{EE} = 0 \tag{5.12}$$

which leads to

$$\Delta I_{c1} = -\Delta I_{c2} \tag{5.13}$$

Substituting the previous expressions into equation (5.9) leads to

$$v_{in1} \Delta V_{b1} = -2\frac{\Delta I_{c2}}{g_m} \tag{5.14}$$

Taking the ratio of equations (5.7) and (5.14) leads to the following expression for voltage gain A_{v12} of a differential amplifier when the output is take from the opposite transistor as the input.

$$A_{v12} = \frac{V_{o2}}{V_{in1}} = \frac{\Delta V_{c2}}{\Delta V_{b1}} = \frac{g_m R_C}{2} \tag{5.15}$$

If the output were to be taken from the collector of Q1 instead of Q2, we could follow virtually the same analysis and would find that the voltage gain A_{v11} would differ only by a minus sign.

$$A_{v11} = \frac{V_{o1}}{V_{in1}} = \frac{\Delta V_{c1}}{\Delta V_{b1}} = \frac{-g_m R_C}{2} \tag{5.16}$$

If we apply a signal to both inputs, and take the output from the collector of Q2, then we can define the differential gain to be

$$A_{dm} = \frac{\Delta V_{c2}}{\Delta V_{b1} - \Delta V_{b2}} = \frac{g_m R_C}{2} = \frac{v_{o2}}{v_{in1} - v_{in2}} \tag{5.17}$$

Input and Output Resistance

The input resistance can readily found by recalling Lab 2, where we showed that the input resistance into a common emitter amplifier was $R_{in} = r_\pi + \beta R_E$. Well, for a diff-amp, the resistance looking into the base of Q1 is $R_{in} = r_{\pi 1} + \beta_1 R'_E$, where R'_E is the effective emitter resistance of Q1. However, this resistance is actually the resistance looking into the emitter of Q2. Recall that the resistance looking into the emitter is $\frac{1}{g_{m2}}$. So, the input resistance looking into the base of Q1 is

$$R_{in} = r_{\pi 1} + \beta \frac{1}{g_{m2}} = r_{\pi 1} + r_{\pi 2} = 2r_\pi \qquad (5.18)$$

So far in these labs we have considered the BJT collector to be a perfect current source. For now let's continue this approximation. So, if we try to drive the output, which is the collector of Q2, with an independent source, all the current will go through R_{C2}. Therefore, the output resistance of the diff-amp is just given by[1]

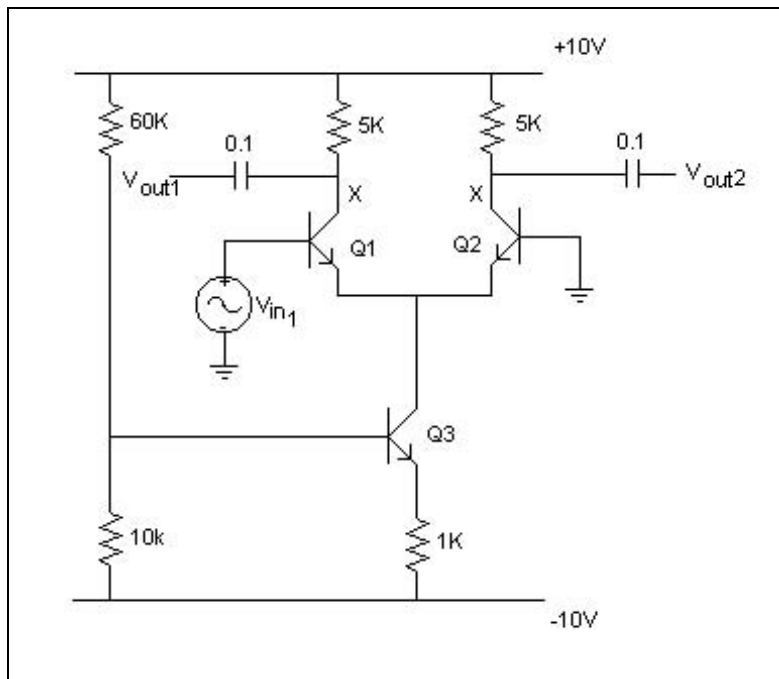$$R_o = R_{C2} \qquad (5.19)$$

5.2.3 Experiment

Figure 5.4: Differential Amplifier for Experiment

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[1]We will find in the next chapter the conditions when we have to consider the output resistance of the collector itself, and the ideal approximation cannot be used.

1. Construct the differential amplifier in Fig. 5.4.

2. Measure the DC values at the collector of Q1 and Q2. Do the measured values agree with theoretical ones.

3. Measure the DC value at the emitter of Q1 and Q2. Do the measured value agree with the theoretical one.

4. Indicate the inverting and non-inverting output.

5. Input an AC signal into Q1 of your circuit at midband frequencies (approximately 50kHz.) What is the single ended voltage gain of your circuit? (You may have to reduce the magnitude of your input signal with a voltage divider to obtain a signal which is small enough that does not clip. If you do use a voltage divider, remember to account for its output resistance, and the input resistance of the circuit, when calculating the gain of the circuit.)

6. By driving the input with sources that have source resistances ranging from 1K to 100K, develop a way to measure the input resistance of the circuit. (Just put resistors ranging from 1K to 100K in series with your signal source.) Does your measured value agree with your theoretical calculation.

7. By driving various AC coupled loads ranging from 1K to 100K, develop a way to measure the output resistance of the circuit. Does your measured value agree with your theoretical calculation.

5.3   Op-Amp Basic Concepts

The circuit in Fig. (5.5) represents a very simple op-amp. It is virtually the same circuit as in the previous section, except there is an emitter follower stage and feedback added. In the circuit, the input signal is applied to Q1. Since the output of the diff-amp is taken from the collector of Q2, the base of Q1 represents the noninverting input. The output of Q2 is then input to Q4 which forms a directly coupled emitter follower stage. The purpose of Q4 is to reduce the output resistance of the circuit. When feedback is applied, a fraction of the output voltage is then fed back to the inverting input (Q2). This provides negative feedback by in effect, reducing the total voltage between the bases of Q1 and Q2.

5.3.1   Open Loop Analysis

Before hooking up the feedback connections, let's perform an open loop analysis of the circuit, which is shown without feedback in Fig. 5.6, starting with the DC bias conditions. The DC analysis is almost the same as before, except now we have to determine the current going through transistor Q4, which gets its bias from V_{CC} through R_{C2} and V_{C2}. Recall from Section 2, that we have established the DC voltages at the collectors of Q1 and Q2, by
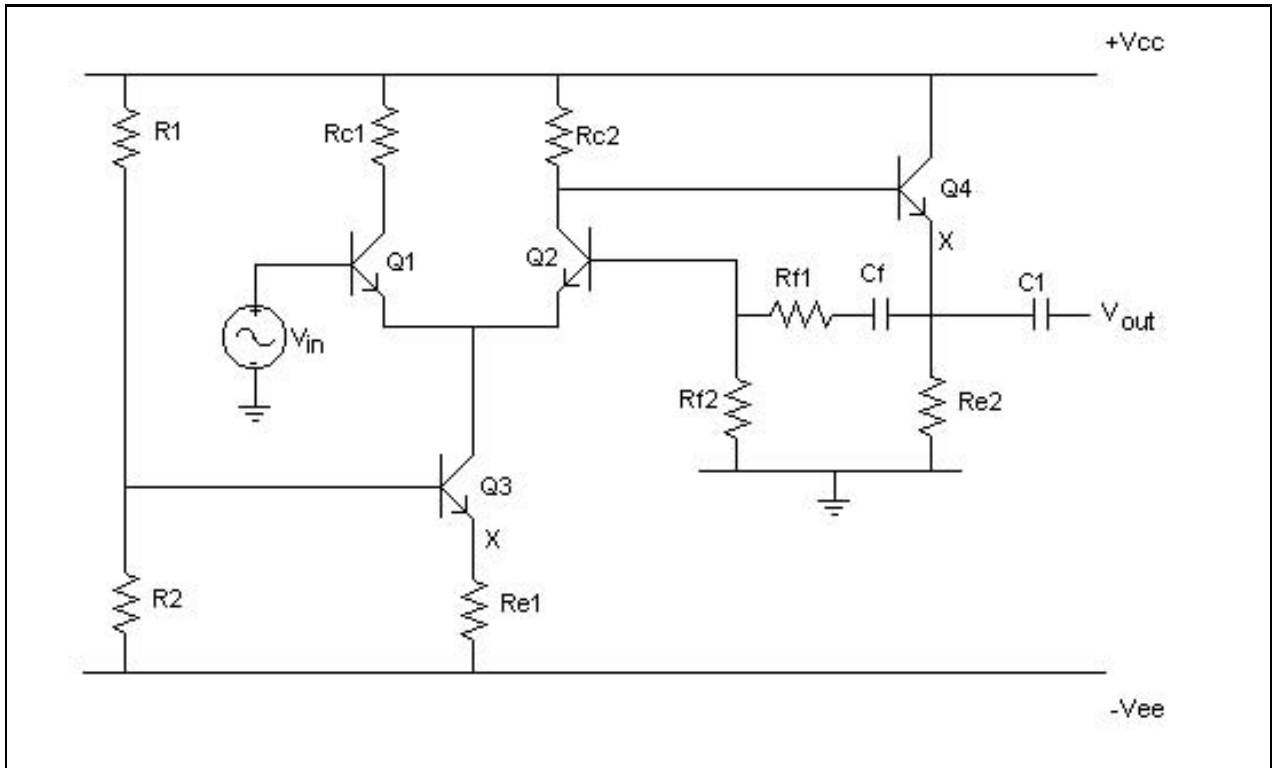
Figure 5.5: Simple Op-Amp-Like Circuit

determining the current provided by the current source Q3, and the determining the drops across R_{C1} and R_{C2}, where

$$V_{C2} = V_{CC} - I_{C2}R_{C2} \tag{5.20}$$

Now that we have added Q4, it would appear as though the DC voltage at V_{C2} would have to be changed to accommodate the current I_{B4}. This would give

$$V_{C2} = V_{B4} = V_{CC} - (I_{C2} + I_{B4})R_{C2} \tag{5.21}$$

However, since β is usually greater than 100, the effective resistance to ground seen by I_{B4} at V_{C2} is βR_{E4}. Since in most cases βR_{E4} is more than 20 times greater than R_{C2}, I_{B4} is negligible compared with I_{C2}, so we can say that even with Q4, V_{C2} is still given by

$$V_{C2} = V_{B4} \approx V_{CC} - I_{C2}R_{C2} \tag{5.22}$$

Now I_{E4} is readily determined by

$$I_{E4} = \frac{V_{B4} - 0.7}{R_{E4}} \tag{5.23}$$

Now that we have I_{E4}, we can approximate $I_{E4} \approx I_{C4}$, and determine $g_{m4} = \frac{I_{C4}}{V_t}$. Using g_{m4} will help determine the small signal output resistance of the circuit.
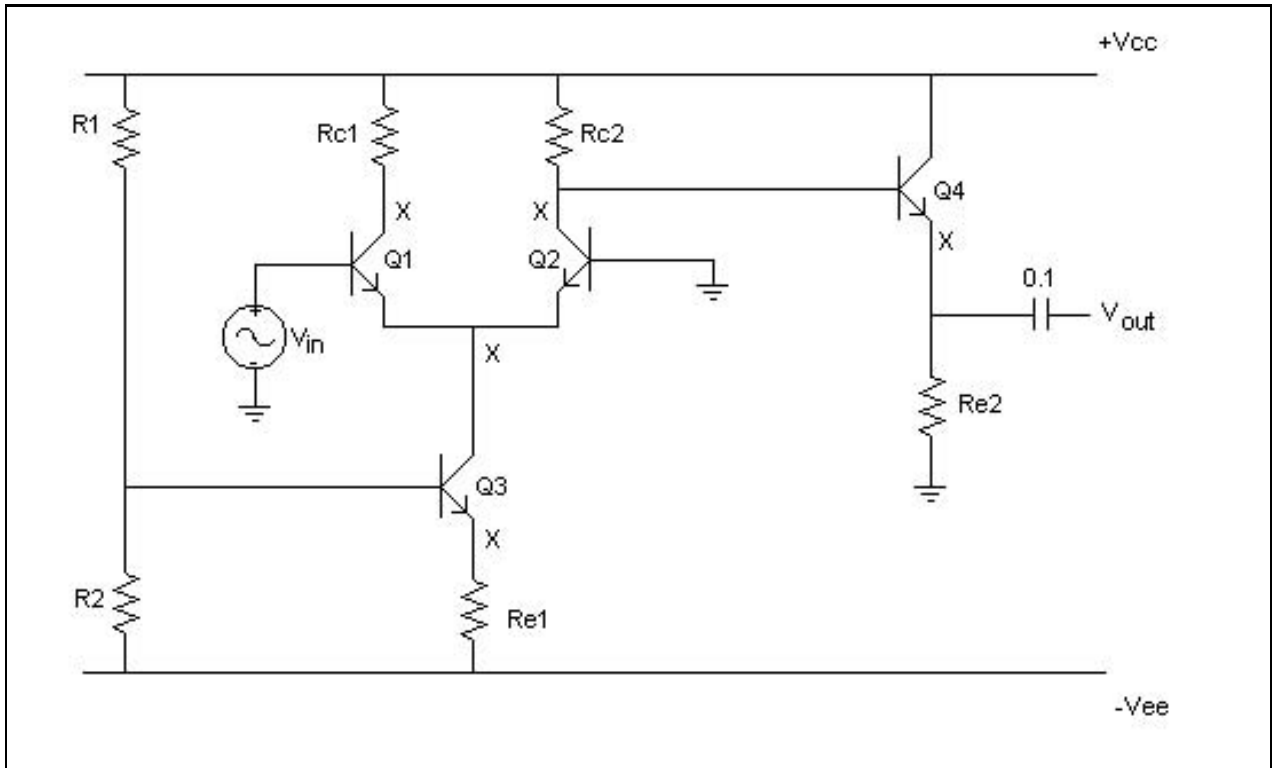
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Figure 5.6: Open Loop Configuration of Op-Amp-Like Circuit

5.3.2   Small Signal Open Loop Gain

To determine the small signal open loop gain we break the circuit up into stages. Looking at Fig. 5.6, we realize that the circuit is composed of a gain stage that is composed of the differential amplifier, and the emitter follower output stage, which acts to lower the output resistance of the circuit. The overall gain of the circuit is then the product of the gain of the two stages:

$$\frac{v_o}{v_{in}} = \left(\frac{\Delta V_{C2}}{v_{in}}\right)\left(\frac{v_o}{\Delta V_{C2}}\right) \tag{5.24}$$

where $\Delta V_{C2} = \Delta V_{B4}$ The approximate result of this calculation can be obtained almost immediately by inspection to be $\frac{v_o}{v_{in}} \approx g_{m2}R_{C2}/2$. Now, let's perform a more detailed analysis to show that this is indeed the case. First of all the gain of the first stage is:

$$\frac{\Delta V_{C2}}{v_{in}} = \frac{g_{m2}R_{C2}||(r_\pi + \beta R_{E4})}{2} \tag{5.25}$$

Where $(r_\pi + \beta R_{E4})$ is the input resistance looking into the base of Q4.

Now, the gain of the second stage is given by

$$\frac{v_o}{\Delta V_{C2}} = \frac{R_{E4}}{R_{E4} + 1/g_{m4}} \tag{5.26}$$

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If we multiply the gain of the two stages together, we arrive at the following expression for the total differential mode gain of the circuit A_{dm}.

$$\frac{v_o}{v_{in}} = A_{dm} = \left(\frac{g_{m2}R_{C2}||(r_\pi + \beta R_{E4})}{2}\right)\left(\frac{R_{E4}}{R_{E4} + 1/g_{m4}}\right) \qquad (5.27)$$

Since R_{E4} is usually much greater than $1/g_{m4}$, in most cases the gain of the second stage can often be approximated by $\frac{\Delta V_{C2}}{v_{in}} \approx 1$. So, the gain of the overall amp is usually given by the gain of the first stage alone described by equation (5.25). Finally, it is often the case that we can neglect $(r_\pi + \beta R_{E4})$ because it is usually much greater than R_{C2}. Under these conditions, the total gain of the circuit can be given by $\frac{v_o}{v_{in}} = A_{dm} \approx g_{m2}R_{C2}/2$, which was mentioned above.

Small Signal Output and Input Resistance

In Lab 2 we showed that the small signal output resistance of an emitter follower circuit is given by

$$R_o = \frac{1}{g_m} + \frac{R'_S}{\beta}||R_E \qquad (5.28)$$

where R'_S is the output or source resistance of the previous stage of the circuit. In our circuit, $R'_S = R_{C2}$, so the output resistance of the circuit is given by

$$R_o = \left(\frac{1}{g_{m4}} + \frac{R_{C2}}{\beta}\right)||R_{E4} \qquad (5.29)$$

The input resistance of the circuit is identical to that of the diff-amp in the previous section of this lab, which is given by

$$R_{in} = 2r_\pi \qquad (5.30)$$

With the small signal input and output resistances, as well as the voltage gain ascertained, we can draw an equivalent circuit for the amplifier.

5.3.3 Gain with Feedback (Closed Loop Gain)

In this section we show how feedback can be used in op-amp-type structures to control and improve circuit performance. The concepts introduced here form some of the basic ideas for op-amp design. The circuit in Fig. 5.5 feeds back some of the output to the inverting input terminal of the diff-amp at the base of Q2. In this circuit we only feedback the AC part because the DC levels at the emitter of Q4 and the base of Q2 are very different due to biasing[2] For now this lab let's consider only midband operating frequencies where the feedback capacitor is a short for AC and open for DC. The effect of the feedback on small

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[2]We well see that in real op-amp circuits this biasing problem is overcome, and DC signals can be fed back as well.

signal gain can be illustrated by the following analysis. We start with the basic open loop gain definition for our circuit, and revise it slightly to account for two inputs (we do not ground the base of Q2).

$$\frac{v_o}{v_{in} - v_2} = A_{dm} \tag{5.31}$$

Where A_{dm} is the differential mode gain given by equation (5.25), and v_2 is the small signal at the base of Q2. Our goal for the analysis will be to eliminate v_2 from the expression, and then determine the closed loop gain $A_{cl} = \frac{v_o}{v_{in}}$. To keep things simple, and illustrate the main points, we will neglect loading effects in our analysis. (This is a good approximation as long as the input resistance into the diff-amp is much greater than the effective resistance of the feedback network, and the resistance of the feedback resistors seen at the emitter of Q4 is much greater than the open loop output resistance of the circuit.) After making these approximations, we can immediately express v_2 in terms of v_o using the expression for a voltage divider and treating the capacitor as an AC short to obtain:

$$v_2 = \frac{v_o R_{F2}}{R_{F1} + R_{F2}} \tag{5.32}$$

Substituting equation (5.32) for v_2 in equation (5.31), and re-arranging gives the following expression for the closed loop gain.

$$A_{cl} = \frac{v_o}{v_{in}} = \frac{A_{dm}}{1 + \frac{A_{dm} R_{F2}}{R_{F2} + R_{F1}}} \tag{5.33}$$

One very interesting aspect of equation (5.33) is that if

$$\frac{A_{dm} R_{F2}}{R_{F2} + R_{F1}} \gg 1 \tag{5.34}$$

then equation (5.33) can be approximated as

$$A_{cl} = \frac{v_o}{v_{in}} \approx 1 + \frac{R_{F1}}{R_{F2}} \tag{5.35}$$

This expression should be recognized as that describing the gain of a noninverting amplifier op-amp circuit. In the final experiment of this lab, you will construct such a feedback circuit, and help determine when equation (5.35) is applicable.

5.3.4 Experiment

1. Set up the circuit in Fig.5.7.

2. Measure the DC values at the points indicated with an 'X'. Calculate the values theoretically and compare them with the measured ones.
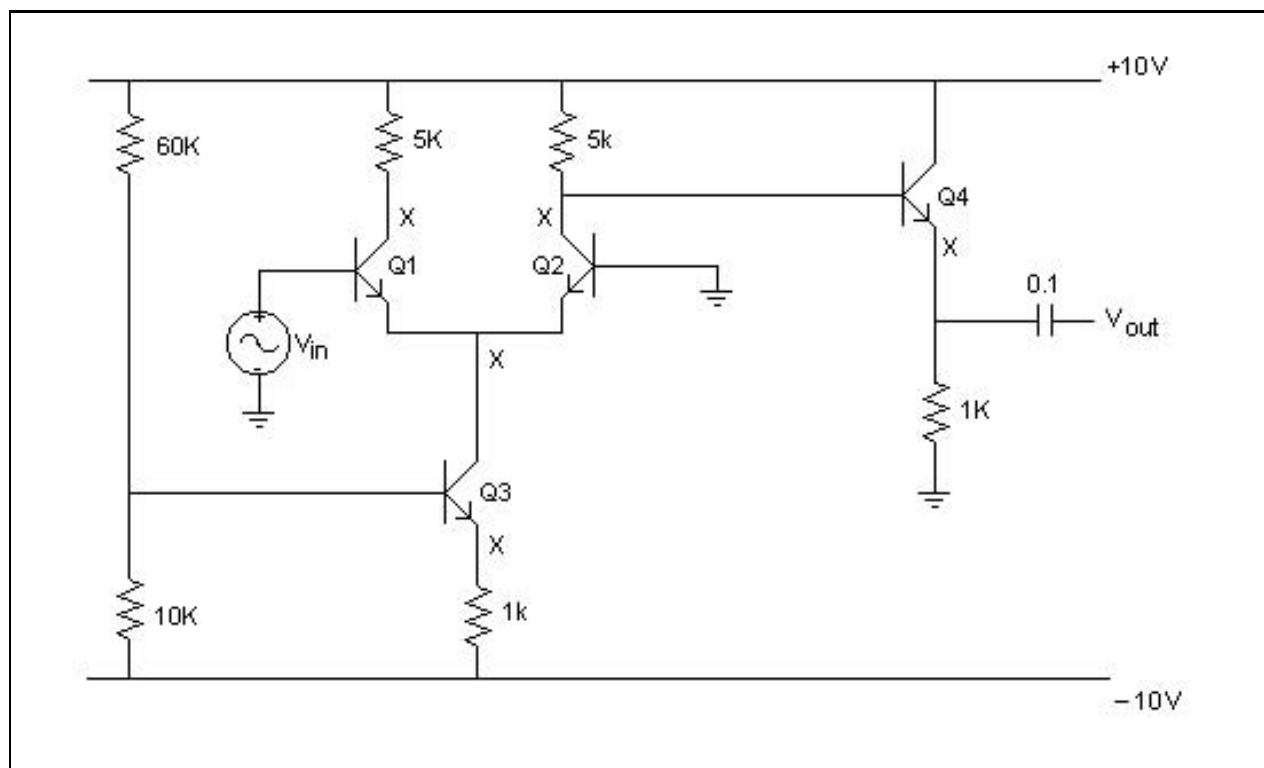
Figure 5.7: Basic Op-Amp

3. Input a sine wave of amplitude 0.03V into Q1. at a frequency of about 50KHz. Measure the open loop voltage gain A_{dm}. Calculate the theoretical value for the gain and compare it to the measured result.

4. By varying the amplitude of the input signal, measure the maximum swing of the circuit. What happens at the output when the input signal becomes too large.

5. By driving several different resistor loads ranging from 100Ω, to 100K, determine the output resistance of this circuit. Compare your measured value with the theoretical one. Also, compare the measured value here with the measured value of the diff-amp in the previous experiment.

6. Connect the feedback as indicated in Fig. (5.5). Use resistance values of 10K and 1K for R_{F1} and R_{F2} respectively, and a $0.1\mu f$. Measure the voltage gain and decide if it can be represented by equation (5.35).

7. By driving various loads like you did above, try to determine the output resistance of the circuit with feedback. How does feedback affect R_o?

5.4   Preliminary Questions

1. For the circuit in Fig.5.4, calculate the DC voltages at the points labeled X, and the small signal voltage gain. Also calculate R_{in} and R_o.

2. For the circuit in Fig.5.7, calculate the DC voltages at the points labeled X, and the open loop small signal voltage gain A_{dm}. Also calculate R_{in} and R_o.

3. For the circuit in Fig.5.7, what feedback resistors would you add for a closed loop gain of 6. (Remember, we want to be able to neglect loading effects from the feedback loop. This limits the size of resistors you can use.)