Laboratory 6

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

6.1 Introduction

In this lab, we will be studying basic MOSFET circuits; we will start with DC biasing circuits then study simple amplifier circuits and finally some applications (e.g. inverters and oscillators).

6.2 The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

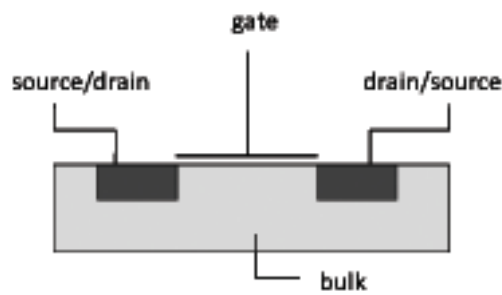The physical configuration we are addressing is shown in Figure 6.1:

Figure 6.1: MOSFET Basic Structure

The source and drain regions are a different semiconductor type than the bulk. In the nMOSFET the source and drain regions are n-type, the bulk is p-type. In the pMOSFET the source and drain regions are p-type, the bulk is n-type. Between the source and the drain is the gate. But the gate is not directly connected to the silicon. Between the gate and the silicon is a very thin silicon-dioxide insulator, which is at the surface of the device.

The NMOSFET works as follows: First, assume the bulk is grounded so $V_B = 0$. Then a positive voltage is applied between the gate and the source, with the gate voltage larger than the source voltage. This pulls electrons out of the source towards the surface of the device. However, since at the surface, below the gate, there is an insulating oxide, the electrons build up along the surface just below the gate and

the oxide. This build-up of electrons forms a conducting channel (which is actually called the 'channel') between the source and drain. The electrons in the channel can then be pulled into the drain by a drain voltage that is higher (more positive) than the source voltage.

The MOSFET is thus called a 'field-effect-transistor' because the gate-source voltage creates an electric field that gives rise to the conducting channel. The concentration of electrons in this channel increases as the gate-source voltage increases. Because of the oxide, there is no current flowing into the gate electrode, only a field, which creates the channel. The drain voltage then pulls the channel electrons into the drain and out of the drain contact to give rise to the drain current I_D. The larger the gate-source voltage, the more electrons there are in the channel, and the higher the drain current. Thus, the drain current is largely dependent on the gate-source voltage. In the saturation region of operation, I_D is almost totally dependent on gate-source voltage V_{GS}, and, to first approximation, does not depend on the drain-source voltage V_{DS} at all. Since in saturation (defined below), the drain current I_D, is dependent on the gate-source voltage V_{GS}, and not on the drain voltage, we call the MOSFET a voltage controlled dependent current source. The minimum value of V_{GS} required to create a channel is called the threshold voltage V_{th}. (*Please, do not confuse the threshold voltage V_{th} in MOSFETs with the thermal voltage V_T in diodes and BJTs*) (The pMOSFET works in an analogous manner but with opposite polarity, and the current carriers are holes, as opposed to electrons.)

The symbol convention for the n-channel device is shown in Figure 6.2.
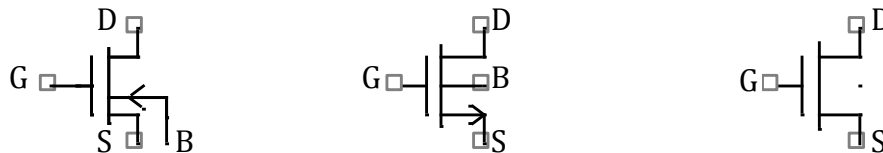

Figure 6.2: n-MOS symbols conventions

There are two main operational modes: saturation, and linear/triode. Our basic configuration and equation for saturation in the nMOSFET ($V_B = V_S$, $V_{GS} > V_{th}$ and $V_{DS} >= V_{GS} - V_{th}$) is:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda \cdot V_{DS})$$

The parameter λ is typically very small and can often be neglected. In this lab, unless said otherwise, assume the parameter λ is zero.

Our basic equation for the linear/triode region in the nMOSFET ($V_B = V_S$, $V_{GS} > V_{th}$ and $V_{DS} \leq V_{GS} - V_{th}$) is:

$$I_D = k_n' \frac{W}{L} [(V_{GS} - V_t)V_{DS} - \frac{1}{2}(V_{DS})^2]$$

Also, for small signal analysis we will need the transconductance g_m.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|I_{DC} = k_n' \frac{W}{L}[(V_{GS} - V_t) = \frac{2I_D}{V_{GS} - V\text{th}} = \sqrt{2k_n' \frac{W}{L} I_D}$$

The DC gate current is 0: $I_G = 0$
The DC source current is equal to the drain current: $I_S = I_D$

As you can see, individual transistors have the parameters: k_n', W, and V_{th}. Remember the symbol convention for the p-channel device:
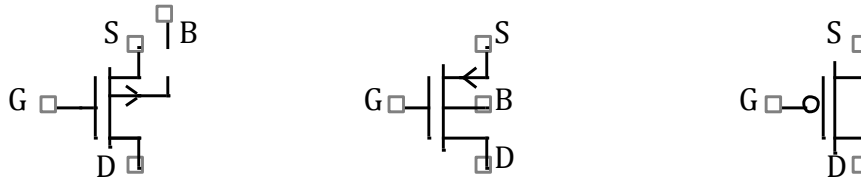

Figure 6.3: p-MOS symbols conventions

For the nMOSFET, when $V_{GS} \leq V_{th}$, we do not have a good channel for current to flow in, but if we had better current measuring equipment, we would notice that there is, in fact, a tiny current that is controlled by the gate voltage. For the purposes of this lab, we will simply call the transistor "turned off".
Life gets more complicated when the bulk and source voltages are not the same (as is typical for integrated circuit design). In DC analysis, we model this as a change in the threshold voltage. This is typically referred to as the "body effect":

$$V_{th} = V_{th0} + \gamma[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f}]$$

where, commonly, $2\varphi \approx 0.7$ V and V_{th0} is the threshold when $V_S = V_B$, both γ and φ_f depend on the doping.

6.3 MOSFET Chip

In this lab you will be experimenting with MOSFETs. The MOSFETs are packaged in a chip shown in Figure 6.4. This pin-out of the HEF4007 chip has been provided to preserve your sanity. More details can be found on the data sheet.
MOSFETs ARE STATIC SENSITIVE ! ! – Please handle with care! Ground yourself whenever handling the pins.
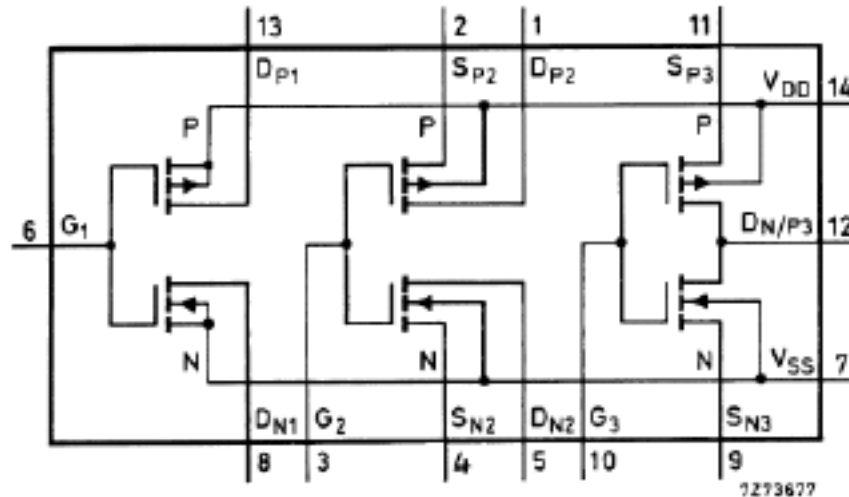

Figure 6.4: HEF4007 Chip pin-out

6.4 Experiment – DC biasing of Common Source

The circuit in Figure 6.5 provides DC bias to an N-channel MOSFET. The two 10K resistors establish a Gate voltage. The Source is connected to a 1K resistor and then to ground. The Gate-Source loop then gives rise to a value for V_{GS} that is greater than the threshold voltage and thus the device will turn on.

In this experiment, we will construct the circuit in Figure 6.5 and verify the calculations you made in the pre-lab. **In the circuit set V_{DD}=9V.**

1. First, we would like to observe the fact that there is virtually no current flowing into the FET gate terminal. First construct just the resistor divider (R3 and R4) and measure the voltage. Now connect the rest of the circuit and measure the gate voltage again. Is it the same?

2. Now measure the voltages at the source and drain. Determine V_{GS} determine the Drain, Source and Gate currents. How well do these match with your prelab calculations? Is the transistor in triode or saturation?
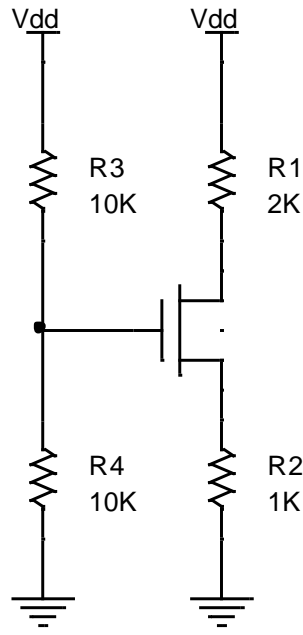
Figure 6.5: Common Source Biasing Circuit

6.5 Experiment – MOSFET Common Source Amplifier

The common source configuration is provided by the circuit in Figure 6.6. With the common source amp, the input is still into the gate (V_G). However the output is taken from the drain (V_D). The gain should be greater than one, and is therefore usually used as a small signal voltage amplifier. (Note that the common source amplifier is analogous to the common emitter amplifier for BJT circuits, in fact their expression for voltage gain is analogous.)

1. Common Source DC Bias Voltage Gain: Measure the DC voltages at the source, drain and gate. Are they what you expected?
2. Common Source AC Voltage Gain: Measure the small signal gain (V_D / V_G). Add a proper capacitor at the output to block the DC. (What value AC coupling capacitor did you use?). Use an input signal of 100mV peak-to-peak at 10 kHz. Is this an inverting or non-inverting amplifier? How does the gain you measured compare with the gain calculated in the preliminary question? If different, explain why?
3. Plotting: Provide a plot of the input *(V_G)* and output *(V_D)* waveforms in your lab report.
4. Increase the bias voltage V_{DD} from 9V to 13.5V, and change the top resistor connected between V_{DD} and the gate from 10K to 20K (just add another 10K resistor in series). What is the gate voltage now? Now measure the voltage gain. What happens?
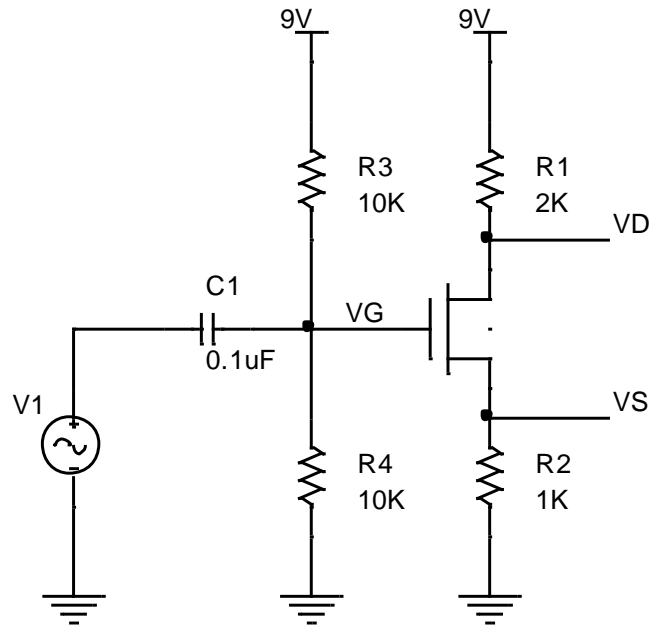
Figure 6.6: Common Source Circuit

6.6 Experiment – MOSFET Source Follower (Also called Common Drain Amplifier)

The source follower configuration is provided also by the circuit in Figure 6.6, with the input into the gate (V_G) and the output is taken from the source (V_S). The gain is less than one, but the benefit of the circuit is that it has a high input resistance and a low output resistance, it is used for driving loads that require significant current while minimizing the sagging of the signal. (Note the similarity between this circuit and the emitter follower for BJT circuits).

1. Construct the circuit in Figure 6.6 and attach an AC coupling capacitor between the source *Vs* and the output *Vo*. Measure the small signal gain, what is the maximum swing for the current configuration?
2. Modify the circuit to obtain the maximum possible swing.

6.7 Experiment – Current Mirror

In this experiment, we will construct the nFET-based current mirror shown in the figure below. In a current mirror, you set the current on the left side of the circuit using KVL and the MOSFET current equations. Then the current on the right side

of the circuit should be the same as the current in the left side. The reason is the VGS is the same for both MOSFETs.
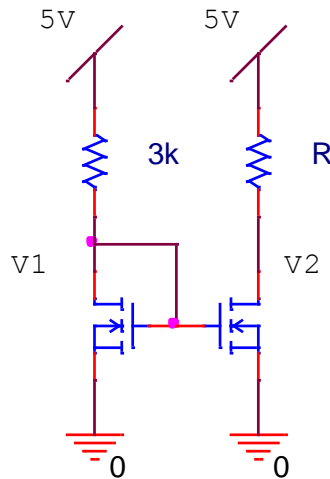
1. Starting with V2 = 5V (R=0), measure the voltage V1 and calculate the current running into the drain of the left-hand nFET. How does this compare with your theoretical prediction?
2. Sweeping V2 from 0V to 5V (by changing R), measure the drain current in the right-hand nFET. Select your own V2 values to obtain a data set that captures all of the features of this curve. (Hint: this means take enough data points so that your plot of ID2 vs. V2 is smooth. Yes, you will be graded on your choice.)
3. The output of the current mirror is not expected to be perfectly constant with changes in V2 due to the Early effect. Using the data you just collected, find the parameter λ.

6.8 Experiment – NMOS Inverter

In this experiment we will look at the NMOS inverter. The inverter works as follows. A voltage is applied to the gate. If the gate voltage (V1 in Figure 6.7) is larger than the threshold voltage V_{th}, the MOSFET turns on and a current flows from VDD, causing a voltage drop across the 10K resistor. As a result, the voltage V2 goes low if the current I_D is large enough (V2= 5V - I_D10K).

1. Construct the circuit shown in Figure 6.7. Sweep V1 from 0V to 5V using step sizes that preserve all of the "relevant" details of the output at V2. You will need to state in your report how you chose the values for V1 with some reasonable justification. Be sure to plot both lines and points for the plot of V2 vs. V1 in your report. (Hint: Take enough points so that the V2 vs. V1 curve looks fairly smooth).
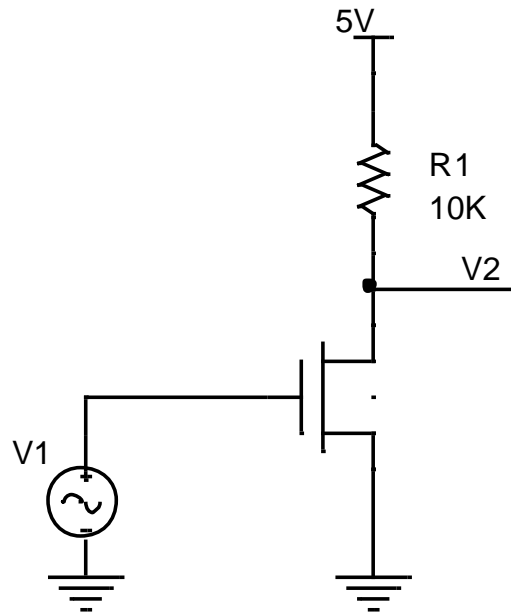
Figure 6.7: NMOS Inverter

6.9 Experiment – CMOS inverter

The CMOS inverter is at the heart of digital electronics. In fact, most logic gates have as their fundamental structure the CMOS inverter. The CMOS inverter has a PMOSFET on top of an NMOSFET. The drains of the two devices are connected together, the gates of the two devices are connected together, while the source of the PMOSFET is connected to V_{DD} and the source of the NMOSFET is connected to ground. Also, the bodies of the respective devices are shorted to their sources as shown. Generally speaking, the CMOS inverter works as follows. When the input V_{in} is Low, (close to zero volts) the PMOSFET is on and the NMOSFET is off. This connects the output to V_{DD} giving a High output. When the input is High, the PMOSFET of off and the NMOSFET is on. This connects the output to ground, giving Low output. In Experiment 6.8, you will investigate the behavior of the CMOS inverter.

In this experiment, we will construct the circuit in Figure 6.8 and verify the calculations you made in the pre-lab.

1. Construct the circuit in Figure 6.8 using V_{DD} = 3.00V as the power supply. Verify that the circuit is acting as an inverter. Using the second power supply, sweep the input voltage from 0 to 3V using 0.2 V steps while recording the output voltage to create a coarse plot of the relationship between Vin and Vout. We would like a lot more detail of the transition of the output voltage from 3V to 0V, so take more points using a 100mV step-size

where the output voltage is between 0.5V and 2.5V. We especially want to know at what input voltage the output is at $V_{DD}/2$. Use the closest point that you have. Plot all of these points on a graph showing *Vout* vs. *Vin*.

2. Set the inverter input (*Vin*) to 0V. Change the power supply to 5.00V and find the inverter threshold voltage again. You do not need to record points, nor plot anything.
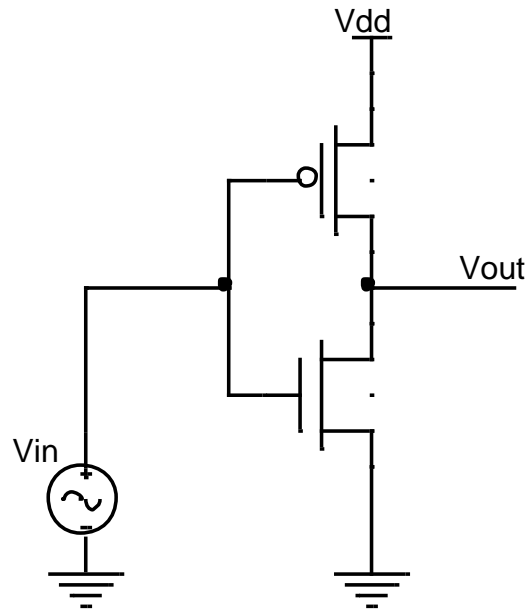

Figure 6.8: CMOS Inverter

3. Change the power supply voltage, V_{DD}, back to 3.00V. Connect a 0.1uF capacitor between *Vout* and ground. We are exaggerating the capacitance that exists in circuits that tend to slow down the logical transition of signals and limit the speed of digital circuits. Use the buffer box (and signal generator) to provide a digital square wave (0V to 3V) to *Vin*. Measure (using cursors) the time it takes for the output to swing from 0V to $V_{DD}/2$ (i.e., propagation delay "tpLH"). Provide a plot of this waveform in your lab report and indicate how you measured this delay. Also measure the time it takes for the output to swing from 3V to $V_{DD}/2$ (i.e., propagation delay "tpHL"). Provide a plot of this waveform in your lab report and indicate how you measured this delay. In your plot, be sure to plot both the input and the output signals.

4. Now measure these two propagation delay values again for the other two inverters that you can make with your HEF4007 chip. Leave the first capacitor on the inverter you just measured and add new capacitors to the two other inverters. Keep these numbers separate, we will be using these six numbers later. For the lab report, what is the mean value of the transition time tpLH? How about tpHL?

5. Change the buffer box input signal to swing between 0V and 5V. Change the power supply providing power for the whole inverter to 5.00V. Once again, measure the time it takes for the output to swing from 0V to $V_{DD}/2$. Measure the time it takes for the output to swing from 5V to $V_{DD}/2$.
6. How do the transition times differ between the 5V supply condition and the 3V supply condition? Why is this?

6.10 Experiment – Ring Oscillator

A ring oscillator is an odd number of inverters connected in series with the output fed back to the input as shown in Figure 6.9. The ring oscillator and its relatives are fundamental circuits used as clocks in computers and carrier wave generators in wireless communications. It is also a fundamental circuit for evaluating the intrinsic speed of a CMOS process. The frequency of oscillation is inversely proportional to the number of stages and the propagation delay times, and is governed by the following:
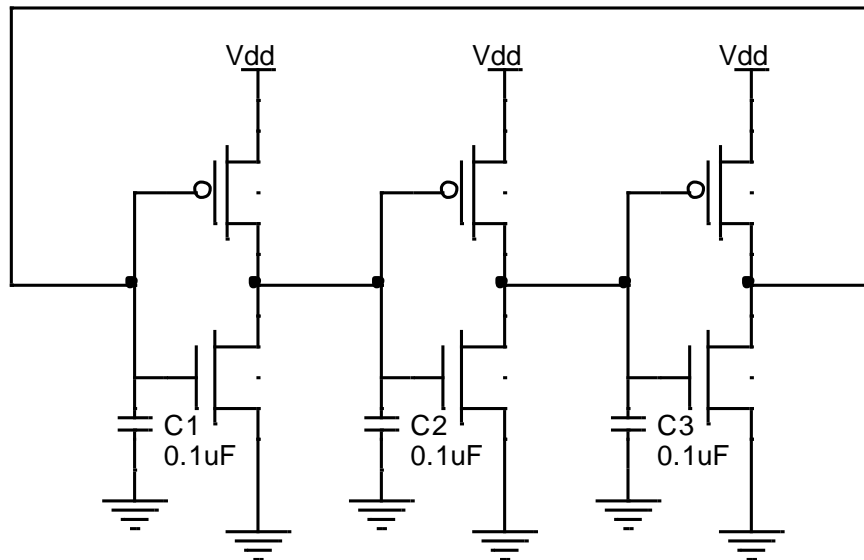
$$F = 1 / (t_{pLH} + t_{pHL}) \, n$$

Figure 6.9: Ring Oscillator

1. Using 3 inverters (each with a 0.1uF capacitor loads), construct the circuit shown in Figure 6.9. Be sure that your power supply voltage is 3.00V. This is a ring oscillator. Measure the frequency by using the frequency measurement function on your oscilloscope. Be sure to have at least 10 cycles of the oscillation on the screen before measuring. To read a measurement, stop the sampling. Restart the oscilloscope measurement for a few seconds, stop it

again, and then record another measurement. Make sure that you are not averaging on the oscilloscope! Calculate the average of 10 measurements as your mean oscillation frequency. How well does your period (1/frequency) measurement correspond to the sum of the inverter transition times measured in experiment 6.8.

2. Change the power supply to 5V and perform the same procedure as in (1) to measure the mean frequency of oscillation. How does this frequency compare with the frequency you obtained in part 1?

3. Reduce the power supply back down to 3V and remove all of the capacitors and measure the mean oscillation frequency of the oscillator again. This frequency is likely to be very high, why do you think this is the case?

Preliminary Questions:

1. Consider a MOSFET operating in saturation whose source is grounded. If we know that we will have 0.6mA flow through it at a V_{GS} of 2.5V, and 8mA flow through it at a V_{GS} of 5V, what is the threshold voltage?

2. What defines the transition from saturation to triode mode?

3. Calculate the DC bias conditions for the circuit in Figure 6.5. Determine V_G, V_S, and V_D. Assume that V_{th} = 1.55V and that $(1/2)k_n'(W/L)$ = 290 micro-amps per V^2.

4. Use the 'delta' method or draw the small signal equivalent circuit for Figure 6.6 and solve for the gain in terms of the variable g_m and the given resistors. Assume that the capacitor C is large enough (when the 10K resistors are considered) to be considered infinite. Assuming that V_{th} = 1.55V and that $(1/2)k_n'(W/L)$ = 290 micro-amps per V^2, solve for the numerical value for the gain. Assume that r_o is infinite. (You will have to find the drain current to solve for g_m. You must show your calculations!) Do this for both the Common Source and the Source Follower configurations.

5. Look at the circuit in Figure 6.6. If this transistor has a V_{th} = 1.55V and we pretend that γ = 0, is the transistor operating in saturation or triode? (Assume $(1/2)k_n'(W/L)$ = 100 micro-amps per $volt^2$.) Explain how we can determine this. Calculate all of the voltages in the circuit. If we are interested in increasing the 2K resistor value to obtain a higher ac gain (when used as an amplifier), what is the largest value we could use and keep the transistor in saturation?.

6. Describe the CMOS inverter circuit (its topology). Then describe the operation of the circuit in words.

7. One way to define the threshold voltage of the inverter is to find the gate voltage for which the saturation currents of the nMOSFET and pMOSFET are equal. If V_{thn} (nMOSFET threshold) = 1.55V and V_{thp} (pMOSFET threshold) = 1.50V and $(1/2)k_n'(W/L)$ =290 μ A/ V^2 and $(1/2)k_p(W/L)$ = 250 μ A/ V^2, find the logic threshold of an inverter made using these two transistors. Take V_{DD} to be 5V. (In practice, things are more complicated and the inverter threshold is usually defined as the input voltage where the output crosses $V_{DD}/2$.)