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ENEE 417 -Spring 2013
Week #5 starting W 02/20/13
Designs #2: Ring and Phase Shift Oscillator Designs; VLSI & Spice Extraction

In this experiment a good reference is Sedra and Smith (pages 1239 & 1345 of the 6th edition) For the active devices use the 4007 CMOS transistor package 1458 Op-Amps.

1. Construct both a three stage and a five stage ring oscillator and record via the GPIB the oscillations. Check the results of Figure 15.28 of the above reference.

Insert various capacitors at the outputs of the stages and see the effects. Among the capacitor values use one of the super-capacitors (whose values are on the order of Farads). Check also the effect of using an even number of stages.

2. Using an Op-Amp amplifier realize the phase shift oscillator of Fig. 17.7 using R=10Kohm and C as 15nFd = 15,000pFd and 18nFd.

Optional but good experience:
3. In Spice use MOSIS 1.6u level 4 CMOS model parameters, available in the bicmos12.lib files, to design a three stage inverter ring oscillator (for this adjust the W and L so that a symmetric bias yields zero output voltage for zero input voltage; make sure that both W and L are bigger than 7microns). Based on your Spice design make a vlsi layout of your three stage ring oscillator. Using the layout obtain a Spice extraction. Insert the models used for your original Spice design and check that your layout gives comparable results to your original design.