ENEE 307
Electronic Circuit Design Laboratory
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A. Iliadis
Electrical Engineering Department
University of Maryland
College Park
MD 20742

Logic Circuits

5.1. Digital Circuits: Read Only Memories (ROMs) and Transistor Transistor Logic(TTLs).

This is a digital application project aiming at understanding the basic and fundamental principles of data storage and logic functions.

Before coming to this lab you should have your PSPICE design ready to show to your TA and have studied Chapter 15 (15.2, 15.5,) Memory Circuits, and , in Sedra and Smith 6th Edition. Include your PSPICE design results in your report.

5.1.1. ROMs.

In digital circuits the devices can have two states: high which corresponds to 1 and low which corresponds to 0, and data are stored on the basis of these two states and their combination. Memories are represented as a two dimensional grid consisting of horizontal and vertical lines, whereby the horizontal lines represent the WORD lines (WL) and the vertical ones the BIT lines (BL). In a ROM cell, the cell is designed so that when the WL is activated the BL shows a 0 or a 1 that was stored, and it always shows the same state when the WL (input) is activated.

Consider a typical ROM cell in Fig. 5.1 a, where the 1 is stored, in the npn transistor connected to the WL by its base and the BL by its emitter, and Fig. 5.1 b, where the 0 is stored by simply omitting the transistor. The collector is connected to the power supply $V_{CC} = 5$ V, and the BL are all clamped resistively to the ground. Therefore, the bit line without the transistor will always be in a low voltage pulled down by the resistor to the ground, while the bit line with the transistor will always have a high when the WL is activated since that turns the transistor on.

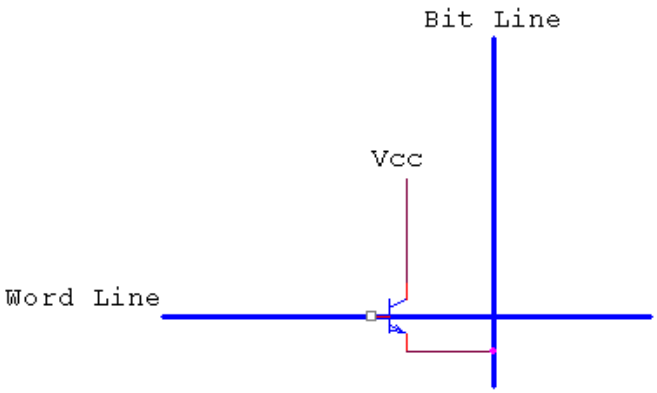

Fig. 5.1 a. 1 bit line.

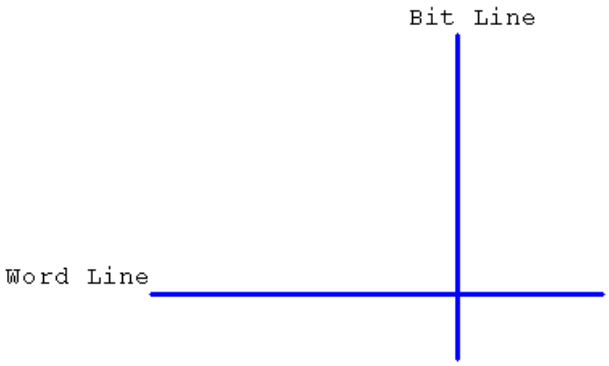

Fig. 5.1.b. 0 bit line.

Since no physical connection exists between the WL and the BL, when the transistor is missing, the 0 BL will always give a low independent of the value of the WL. On the other hand, when the WL is addressed with a high (V_{WH}) and there is a transistor, then the BL is pulled up to $V_{BH} = V_{WH} - V_{BE}$, resulting in 1.

Since in large ROMs the BL can extend several hundred microns, their capacitance is non-trivial and the transistor needs to provide current to charge the capacitance of the BL for the memory to work properly.

In this project you will build a 4X4 bipolar transistor ROM cell array using the 3904 npn bipolar transistors, with the BL resistivelly clamped to the ground. In order to be able to retreive your data from your memory a sensing amplifier is needed, but we will do it optically by sensing the light coming from a light emitting diode (LED). When the LED is on then this BL is a 1, and when it is

off the BL is a 0. Fig. 5.2, shows a 4X4 ROM cell.

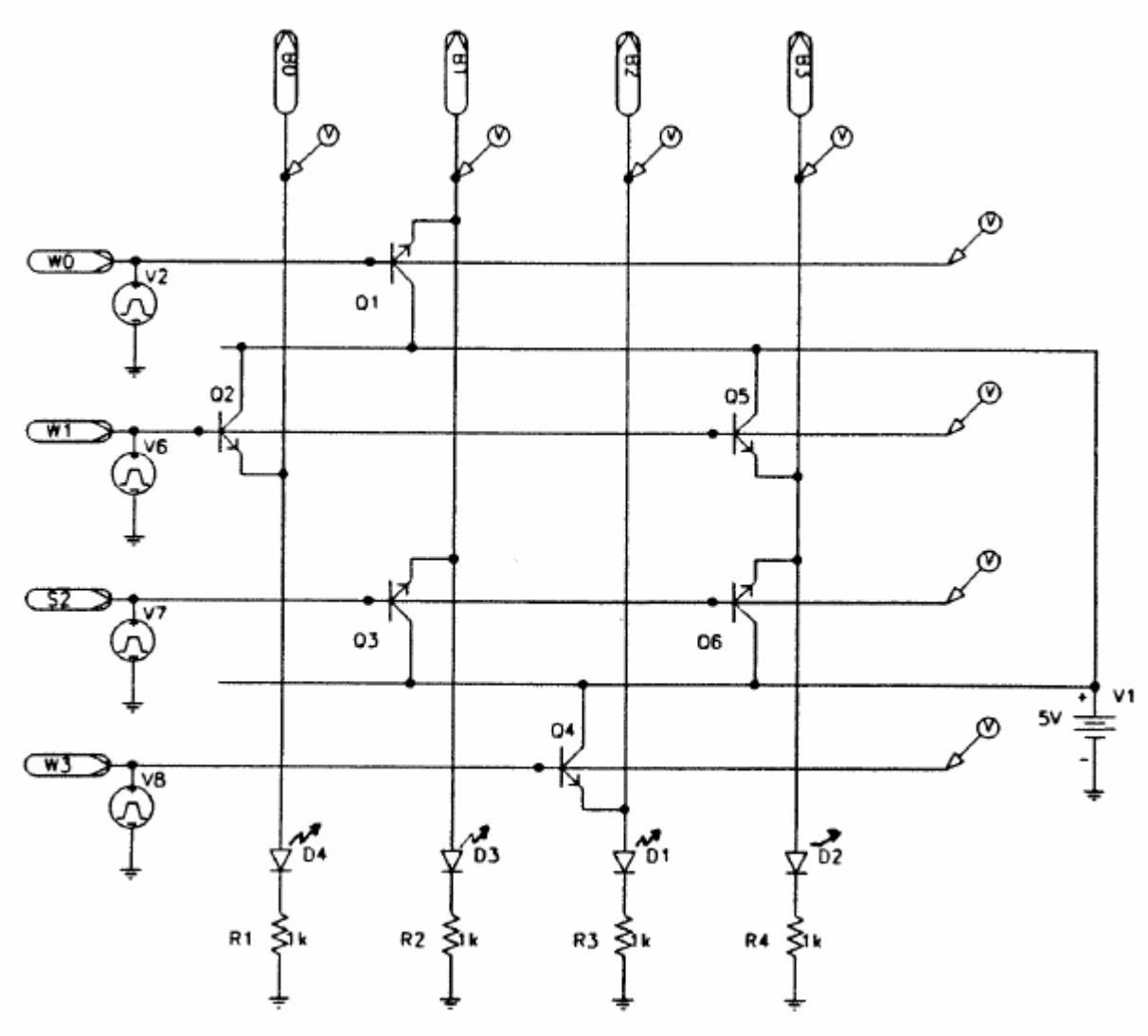

Fig. 5.2. 4X4 ROM array.

5.1.2. Tasks.

1. Use SPICE to design your ROM cell, with various transistor combinations, and define the zeros and ones taking into account all voltages and using a $V_{CC} = 5$ V power supply for your memory. Find the switching speed of your memory in SPICE.

2. Test and measure your memory. Test it using the LEDs. Measure voltages, and switching speed by increasing the frequency of the input signal. Also see when the LED stop following the WL changes, meaning that they cannot switch fast enough. This may mean that your LEDs are slow and your memory is faster or you reached the switching speed of your memory?
What are the factors affecting memory speed?

5.2.1. NAND Gate Design.

A NAND gate is a logic element that has two inputs A and B and one output C and produces an output 1 or 0 depending on the combination of 1's and 0's at the inputs. A truth table is given below in Fig. 5.3 along with the logic symbol of the NAND gate. As you can see the NAND gate provides a 0 at the output only when both inputs are 1.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 5.3. NAND Gate Symbol and Truth table.

In order to build a NAND gate we use two input transistors Q7, Q8 and two output transistors Q9, Q10 as shown in Fig. 5.4. Again an LED is used in the collector of Q10 to indicate the state of the output.

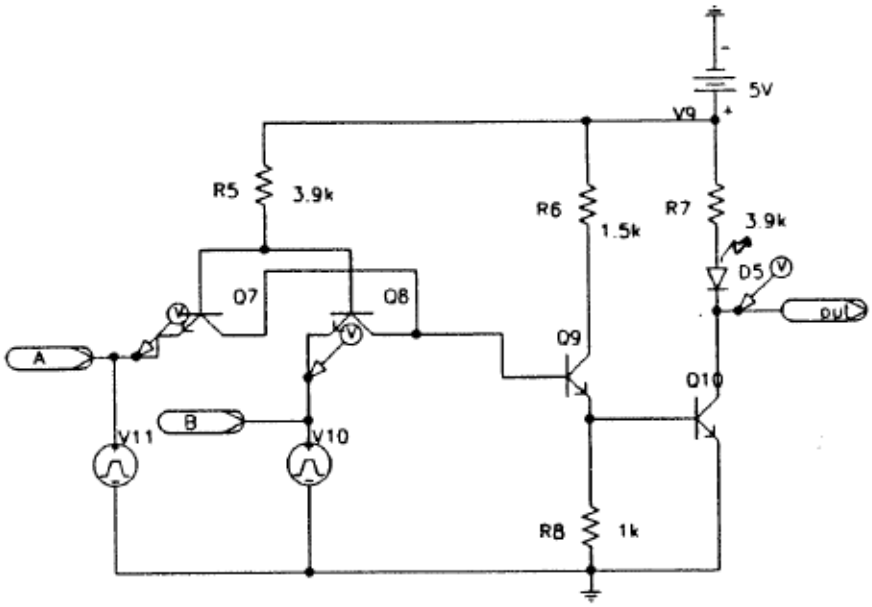

Fig. 5.4. NAND gate circuit.

5.2.2. Tasks.

1. Use SPICE to design the NAND gate. Choose reasonable values for the resistances and incorporate the LED in the circuit. Input two step signals and obtain the output signal to verify your truth table. Test the response speed of your gate by increasing the frequency of the pulsed inputs.

2. Build the NAND gate and test its logic function by observing the LED. Measure voltages and the response speed of your gate.

3. **Extra Credit.** Feel free to make another type of a logic gate following the same methodology and using a different truth table.