ENEE 307
Electronic Circuit Design Laboratory
Spring 2012

A. Iliadis
Electrical Engineering Department
University of Maryland
College Park
MD 20742

Video Amps

2.2. Video Amplifiers

Before coming to this lab you should have your PSPICE design ready to show to your TA and have studied Amp Frequency Response and Feedback in Sedra and Smith 6th Edition. Include your PSPICE design results in your report.

2.2.1. Video Amps.

Video Amps are wide-bandwidth amplifiers working in the frequency range between 1 KHz and 30 MHz and they are capable of linear amplification with reasonable gain but not necessarily much power since they do not need to drive any speakers. Although one can make a very sophisticated Video Amp with several stages of pre-amplification and amplification, the most simple designs are usually more than adequate and consist mainly of an input double stage differential amplifier for the voltage gain necessary and an output stage amp, usually in emitter-follower configuration. In order to increase the bandwidth of the amplifier the gain must be reduced, which requires negative feedback. Feedback from the output to the second differential stage is one necessity, and feedback by introducing emitter degenerative resistors in the first differential stage is another.

Fig. 2.2.1. Shows a schematic of the video amp. As you can see it is very similar to the two stage diff amp of project #1. Here the specifications call for linear amplification especially in the 5 to 7 MHz region necessary for video applications. This amplifier can also be used at lower frequencies and higher gain/power for RF amplification in your Radio project #3.

In the first part of this Lab you may use the double stage Differential Amplifier from project #1, and design a final output power stage to deliver the necessary current to drive the speakers, or you can redesign the pre-amp stage if its performance was far below specs. This stage is important as it decides the total harmonic distortion (THD) of your audio amp and hence its HiFi quality. THD must usually be below 1% for HiFi results. The 2N2222 (or 3904-6) BJT will be your active transistor element and you may choose any passive component values (resistors, capacitors etc) you deem appropriate to make your circuit work under the given specifications.

For this project your task is to have a linear amplifier at 5 to 7 MHz with a reasonable gain around 50 or more.

2.2.2. Frequency Response.

Starting from the single transistor amplifier in common-emitter mode (Fig. 2.2.2), high frequency operation is affected mostly by intrinsic transistor parameters such as the capacitances of the junctions, the base resistance, as well as the source resistance and load resistance and capacitance. An expression for the gain is given as:

$$A_V = [- g_m G_1]/[G_L + j\omega(C_{cb} + C_L)][G_1 + j\omega(C_{be} + C_{cb} + g_m R_L C_{cb})] \quad (2.2.1).$$

Where:

$G_1 = 1/(R_s + r_b)$ the source and base input resistance,

$G_L = 1/r_0 // R_L$ the output and load resistance,

C_{cb}= collector-base juction capacitance (the Miller capacitance C_μ),

C_{be}= base-emitter capacitance (the C_π)

and the usual meening for the rest.

We will define two radian frequencies now as:

$$\omega_1 = 2\pi f_1 = G_1/[C_{be} + C_{cb} (1+ g_m R_L)] \quad (2.2.2)$$

$$\omega_2 = 2\pi f_2 = G_L/[C_{cb} + C_L] \quad (2.2.3)$$

Then Eq (2.2.1) can be written as:

$$A_V = [- g_m R_L]/[1 + j(\omega/\omega_1)][1 + j(\omega/\omega_2)] \quad (2.2.4)$$

Therefore the transistor has two breakpoint frequencies of which f_1 is usually the smaller and hence the one controlling the frequency responce of the amplifier.

Unity Gain Frequency is defined as that $\omega=\omega_T$, where the short-circuit (R_L=0) gain $A_V(sc) = 1$.

Given:

$$A_V(sc) = \_/[1 + j\omega_T\{(C_{be} + C_{cb})/(g_m/\_)\}] = 1 \quad (2.2.5)$$

then since $\_ >> 1$ (2.2.5) gives:

$$\omega_T = g_m/[C_{be} + C_{cb}] \quad (2.2.6)$$

Hence ω_T is a good parameter to identify the max operational frequency of the transistor.

2.2.3. Biasing Circuit.

Fig. 2.2.3 shows the biasing circuit of your amplifier. Q_8 is the biasing transistor in diode connected mode, distributing the current into the other current mirror branches. Assuming your design is set for a power source of $V^+ = +9$ to $V^- = -9$ V, then to set your dc biasing conditions you may start with Q_8. That is assume you put $R_8 = 15$ K, then $I_8 = (18\text{-}0.7)/(15+2.3) = 1$ mA biasing current for $R_8' = 2.3$K. Now you know the voltage drop accross R_8' is 2.3 V and therefore all the other emitter resistances in the branches will have to have the same voltage drop i.e. R_7, R_9, R_{10}, and R_{11}, will have 2.3 V accross so if you choose $R_7 = 500\ \Omega$, then $I_7 = 2.3/0.5 = 4.6$ mA which is a reasonable current for that branch. Same for $R_9 = 500$ and $I_7 = I_9 = 4.6$ mA. $I_{10} = I_{11} = 2.3/700 = 3.3$ mA, for $R_{10} = R_{11} = 700\ \Omega$. This should give you reasonable biasing for your transistors. You may however, wish to run more or less current through the transistors, so your calculations should be along the same lines but with different values.

Now that you have all the currents in the branches, for example in the first stage diff amp each branch will have 4.6 mA/2 = 2.3 mA etc, the ac gain analysis can be done.

2.2.4. AC Gain Analysis.

To perform the gain analysis we take advantage of the symmetry of our circuit and just do the analysis on half of the circuit as shown in Fig. 2.2.4. As we decided to introduce emitter resistances in the **first stage** diff amp, then the dynamic transfer conductance g_m is now redefined as g_{fe} (emitter feedback) and given by:

$$g_{fe} = g_{m1}/[1 + g_{m1}R_E] = 1/[(V_T/I_C) + R_E] \qquad (2.2.7)$$

Obviously $g_{fe}=g_{m1}$ when $R_E = 0$.

The voltage gain produced by each half of the **second stage** diff amp Q_3 and Q_4 is:

$A_{V2} = - g_{m2} R_3 = [4.6/2]/[0.026] \times R_3$ = something a little over 100 so $R_3 = 1$ to 1.2 K say 1.1 K.

So $A_{V2} = - 110$ (2.2.8)

The voltage gain by each half of the **third stage** emitter follower output Q_5 and Q_6 is:

$$A_{V3} = R_L/ [R_L + (V_T/I_C)] = R_L/[R_L + (26/3.3)] = R_L/[R_L + 7.9\ \Omega] \qquad (2.2.9)$$

Which for any reasonable $R_L > 7.9\Omega$ becomes equal to one. Therefore the combined second-third

stage gain is:

A_{V2}x A_{V3} = - 110

Now we can now write a node-voltage equation at point X to connect overall input output with the feedback, as:

$$- g_{fe}(V_{IN}/2) + (V_{OUT}/2)/R_5 - V_X [1/R_1 + 1/R_5] = 0 \qquad (2.2.10)$$

Take $V_{OUT}/2 = A_{V2}xA_{V3}xV_X = - 110V_X$

Then (2.2.10) gives:

$A_V = V_{OUT}/V_{IN} \approx g_{fe}R_5$

and since g_{fe} is given by (2.2.7) the overall gain is given as:

$$A_V = V_{OUT}/V_{IN} \approx g_{fe}R_5 = R_5/[R_E + 26/2.3] = R_5/[R_E + 11\Omega] \qquad (2.2.11)$$

2.2.5. Design Approach.

1. Choose your resistor values for your video amp along the lines described above. Use PSPICE to do the analysis and obtain the characteristics of your amp optimizing linearity for the 5 to 7 MHz region. Maintain a reasonable gain at or above 100 for that range and describe your efforts and results in your report.

2. Realize your chosen circuit on the bread-board. Measure the characteristics of you circuit again and compare with the theoretical characteristics from your PSPICE design. Comment on possible differences between theoretical and measured values in your report.

3. Optimize your video amp for a RF range of 0.5 to 2 MHz. Indicate how you can increase its performance and describe it in your report.

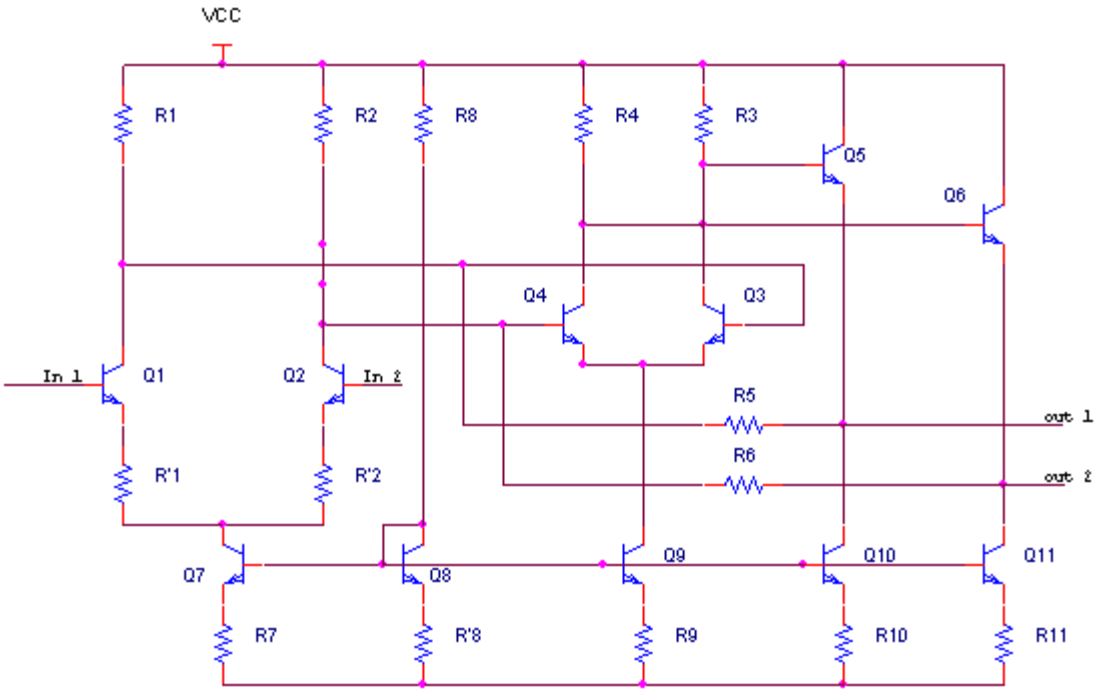

Figure 2.2.1.

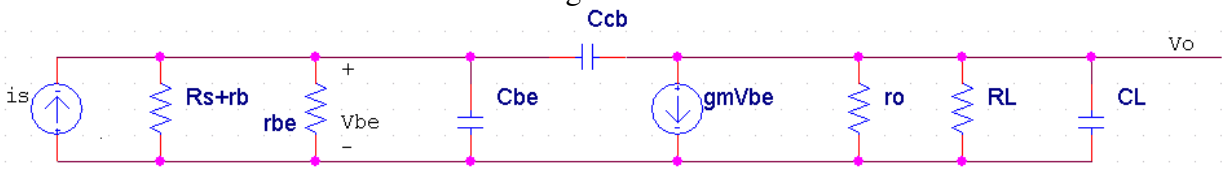

Figure 2.2.2.

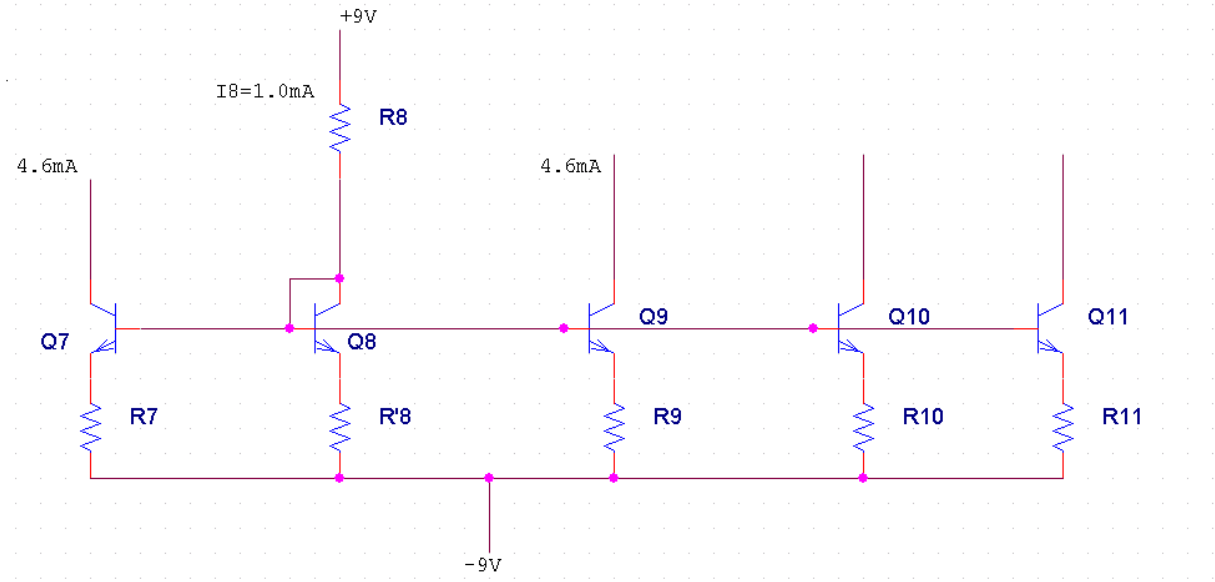

Figure 2.2.3.

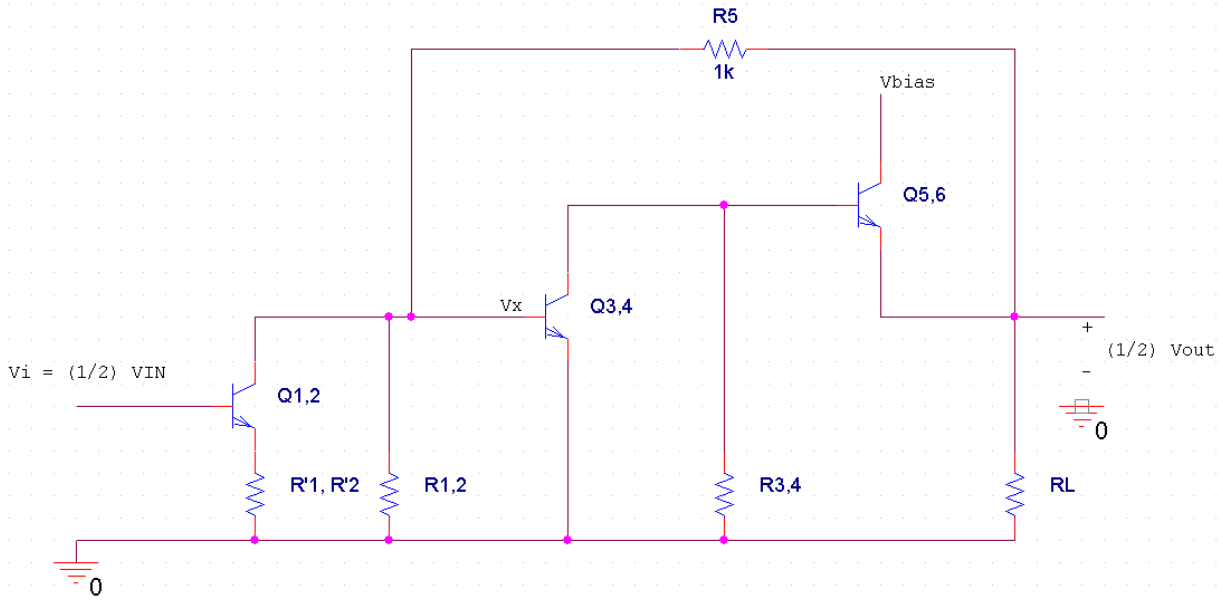

Figure 2.2.4. Half circuit analysis (AC). For half circuit analysis either Q1 or Q2 transistors are used due to symmetry.