ENEE 307
Electronic Circuit Design Laboratory
Spring 2012

A. Iliadis
Electrical Engineering Department
University of Maryland
College Park
MD 20742

Differential Amplifiers

1.1. Differential Amplifiers

Differential amplifiers are the heart of most circuits today and can be used as pre-amplification stages, Op-Amps, modulators-demodulators, sensor elements etc.

Before coming to this lab you should have your PSPICE design ready to show to your TA And have studied Differential Amps in Chapter 8 (pp 612-628, 644-650) of Sedra and Smith 6th Edition. Include your PSPICE design results in your report.

In this Lab you are required to design using SPICE a single stage and a double stage differential amp, build the circuit, and measure the characteristics of the final version of the circuit. The 3904 npn BJT will be your active transistor element and you may choose any passive component values given by PSPICE (resistor, capacitors etc) and that you deem appropriate to make your circuit work under the given specifications.

The diff amp generates an output signal proportional to the difference between the two independent input signals. It consists basically of two MATCHED transistors biased by a current source which is another transistor usually part of a current mirror, as shown in Fig. 1.1. It is important therefore, when you build your circuit to make sure that you use two transistors with closely matched betas. This you will accomplish by measuring the transistors characteristics in the curve tracer or by simply using a multimeter to measure beta.

Before coming to the lab, study the diff amps and current mirrors in the reference books of your course outline. Then use SPICE at the lab to design your circuit. Produce theoretical (PSPICE) input-output signal characteristics using sinusoidal signals, single ended output differential and common mode gains, differential output differential and common mode gains, and the common mode rejection ratio CMRR. Realize your circuit and measure same quantities as above. Compare your theoretical and experimental results. Explain discrepancies.

Reviewing the definitions of the diff-amp parameters, v_1 and v_2 input voltages can be expressed in differential and common mode as:

$$v_{id} = v_1 - v_2 \quad \text{and} \quad v_{ic} = [v_1 + v_2]/2 \qquad [1.1.1]$$

And it follows that for pure differential input (i.e. $v_{ic} = 0$) $v_1 = - v_2$, and for pure common mode input (i.e. $v_{id} = 0$) $v_1 = v_2$.

The gain expressions are derived the usual small signal linear analysis, and once the gains are known then the output voltages can be found for any combination of v_1 and v_2.
Two different types of gain can be extracted:
1. The single-ended differential mode output gain A_{d1} and A_{d2} , measured at each output terminal and the ground is given as:

$A_{d1} = - g_m R_C/2$ and $A_{d2} = + g_m R_C/2$ [1.1.2]

The single-ended common mode output gain A_{c1} and A_{c2} , measured at each output terminal and the ground is given as:

$A_{c1} = - [g_m R_C]/[1+2\, g_m r_{oc}]$ and $A_{c2} = - [g_m R_C]/[1+2\, g_m r_{oc}]$ [1.1.3]

where r_{oc} is the resistance of your current bias i.e. the resistance of transistor Q_3 of the current mirror.

2. The differential (measured between the two output terminals) differential mode output given as:

$A_{dd} = A_{d1} - A_{d2} = g_m R_C$ and [1.1.4]

the differential (measured between the two output terminals) common mode output given as:

$A_{cd} = A_{c1} - A_{c2} = 0$ [1.1.5]

[1.1.4],[1.1.5] are valid only if the two collector resistances are exactly equal.

The primary function of the diff-amp is to enhance the difference between the two inputs and supress the common mode component. Hence a figure of merit for the diff-amp is the common-mode rejection ratio which must be as large as possible and it is defined as follows:

$CMRR = 20\log|A_d|/|A_c|$ [1.1.6]

1.2. Single stage diff-amp.

1.2.1. Design and build a single stage diff-amp (Fig. 1.1) with a linear output response in the frequency range of 20Hz to 20KHz. Use $V_{CC} = 10V$ and $V_{EE} = -10V$.

1.2.2. Measure voltages and currents, diff and common mode gains, open and closed circuit gains, CMRR, and frequency response.

1.2.3. What can you change in the simple circuit to significantly improve its gain? (Current mirror active load).

1.3. Multistage diff-amp.

1.3.1. Design and build a two stage diff-amp (Fig. 1.2) with a linear output response in the frequency range of 20Hz to 20KHz. Target a minimum open circuit voltage gain of 1000 V/V, and a closed-circuit gain of 100 V/V. Design for low power consumption.

1.3.2. Measure the parameters of your circuit as above.
1.3.3. What approach would you take to increase the frequency range of your diff-amp?

1.4. Design a simple op-amp.

1.4.1. Design and build a simple op-amp circuit (Fig. 1.3) with the same specs as your single stage diff-amp.

1.4.2. Measure the parameters and characteristics of the op-amp.

1.5. Extra credit:

1.5.1. Design and build a non-inverting Miller integrator: $v_o(t)$ = 2/RC_$v_i(t)$ dt.
1.5.2. Design and build a full-wave rectifier.

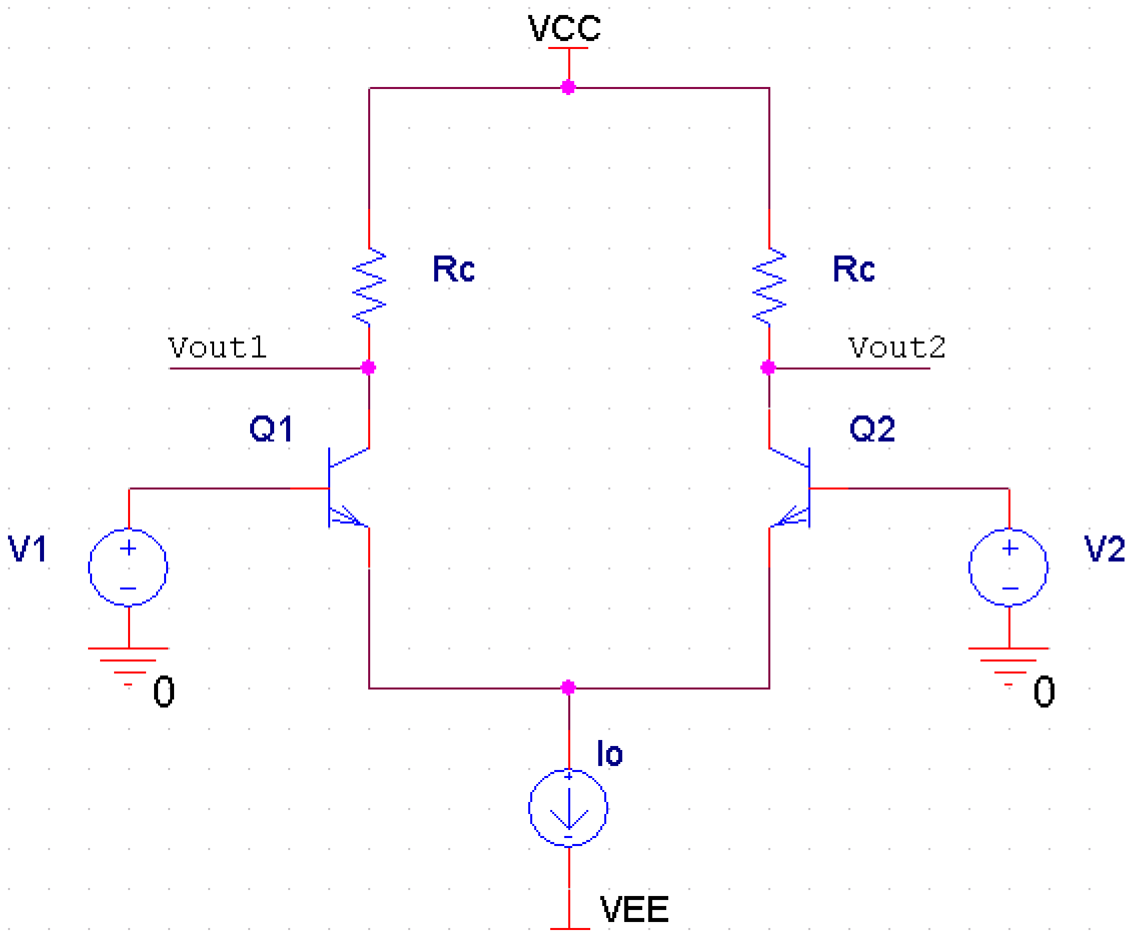

Figure 1.1.

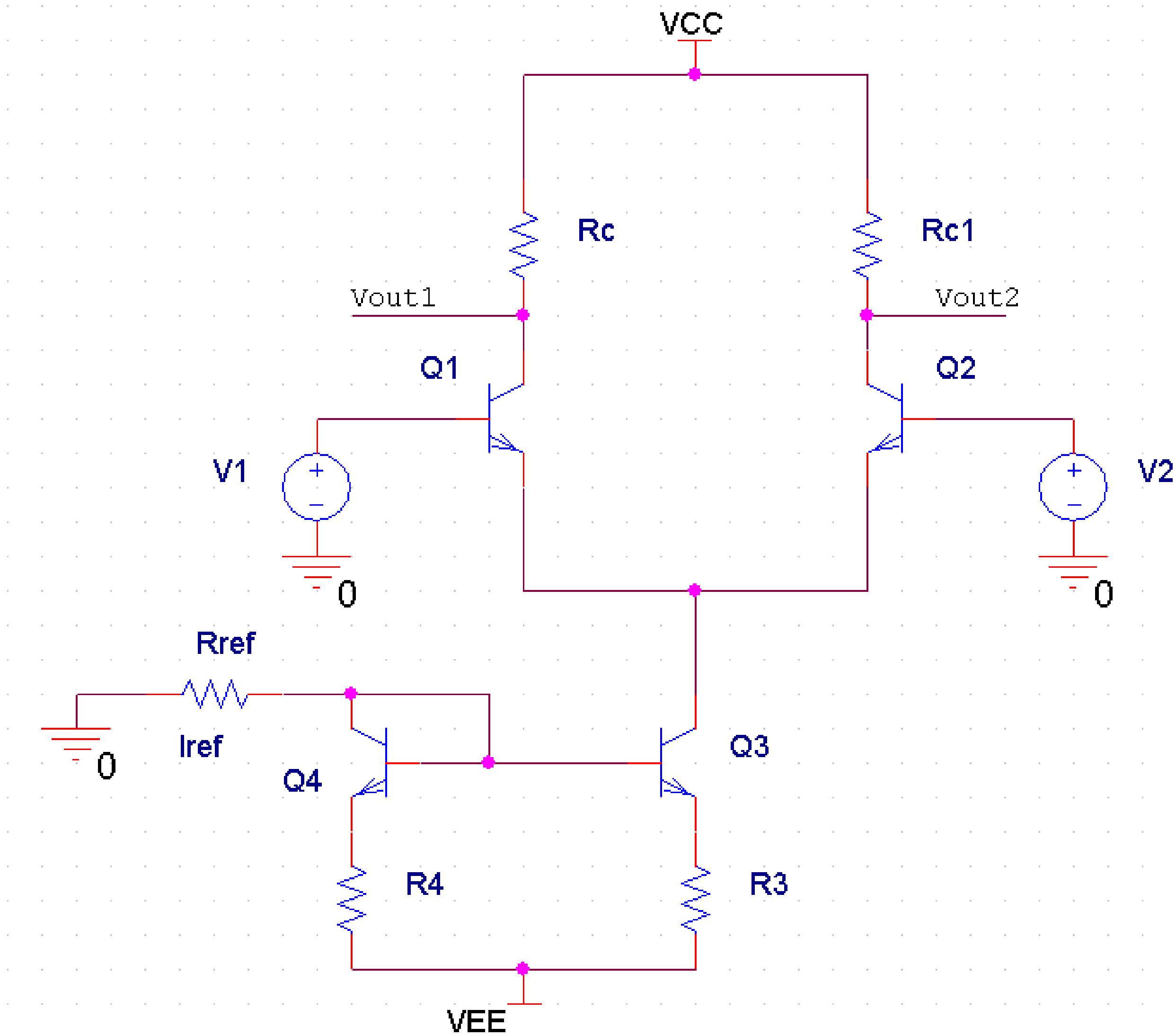

Figure 1.1.2.

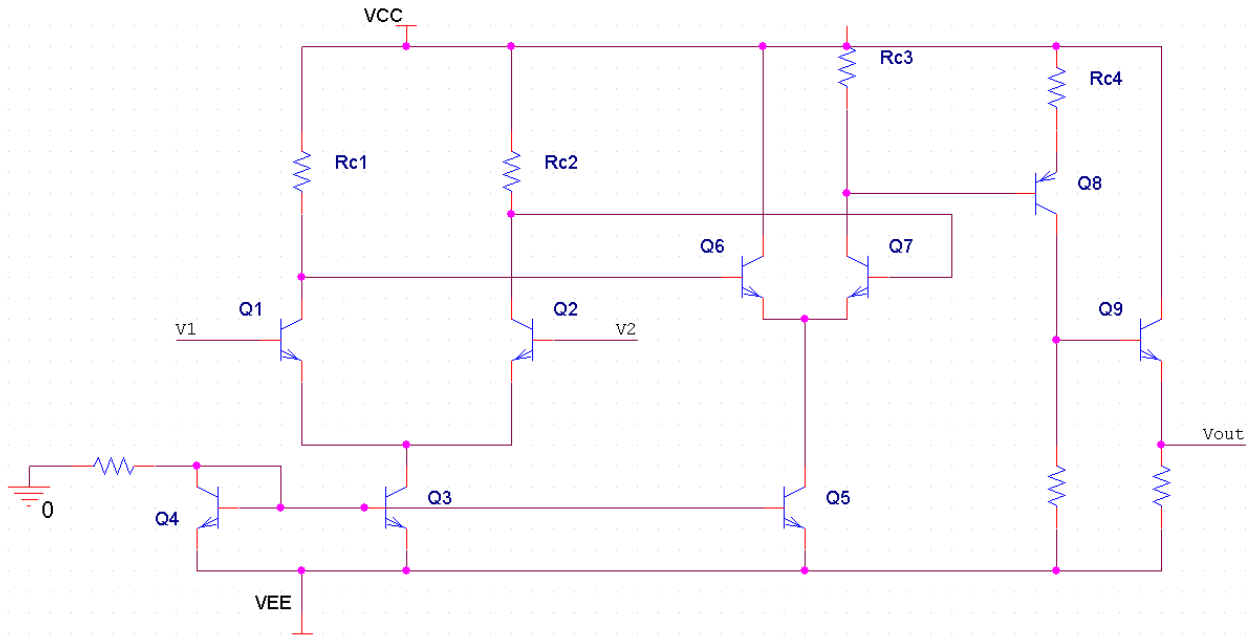

Figure 1.2.

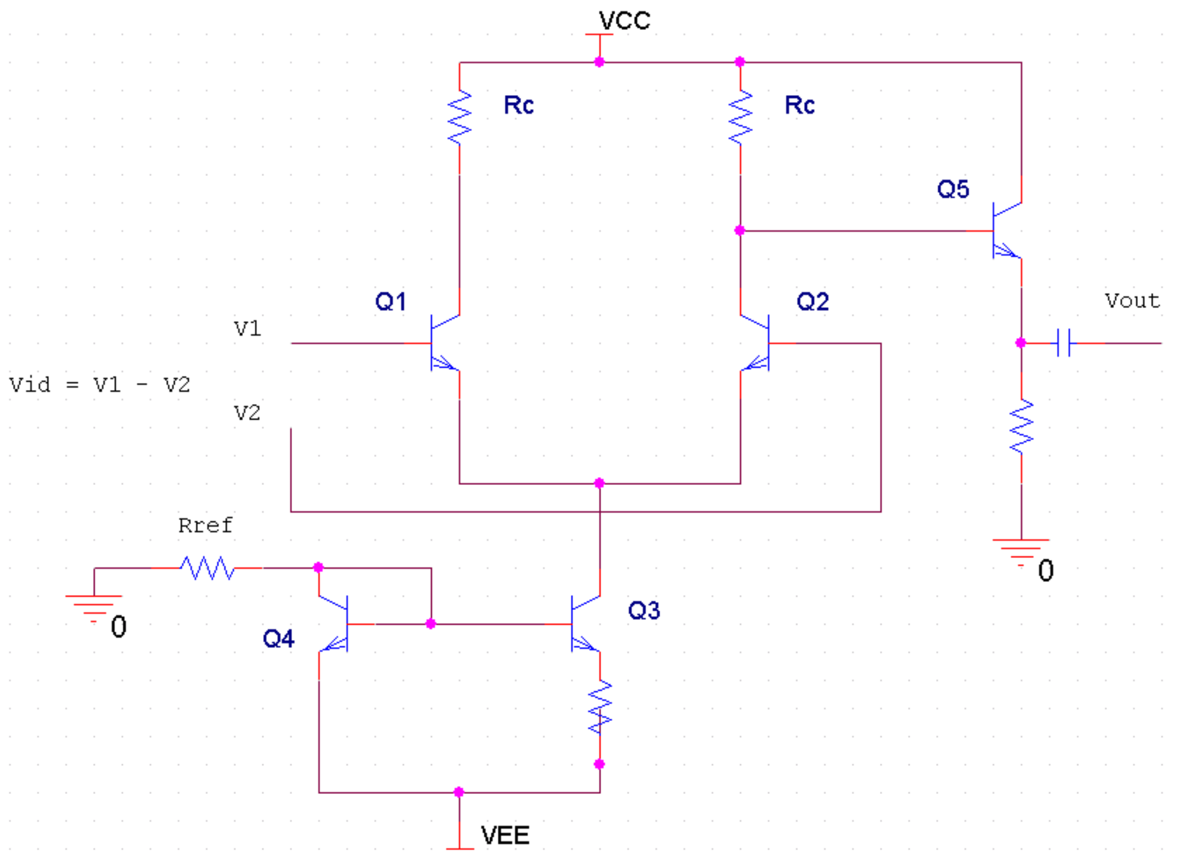

Figure 1.3.