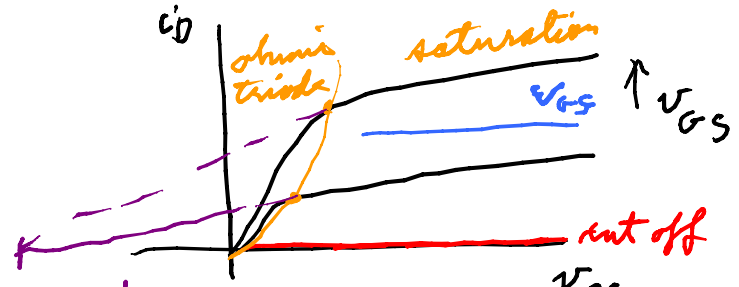
EE303
02/06/12

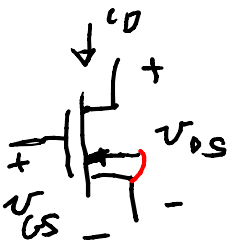
Note Title 2/6/2012

MOS regions



$-V_A = -1/\lambda$ = LAMBDA

V_A is the Early voltage



NMOS

$0 < VTO \Rightarrow$ enhancement mode

$$i_D = \frac{KP}{2}\cdot\frac{W}{L}\begin{cases} 0 \\ [2(v_{GS}-VTO)v_{DS} - v_{DS}^2](1+\lambda v_{DS}) \\ (v_{GS}-VTO)^2(1+\lambda v_{DS}) \end{cases}$$

$v_{GS} - VTO \le 0 \le v_{DS}$ cut off

$0 \le v_{DS} \le v_{GS} - VTO$ (triode)

saturation

$0 \le v_{GS} - VTO \le v_{DS}$

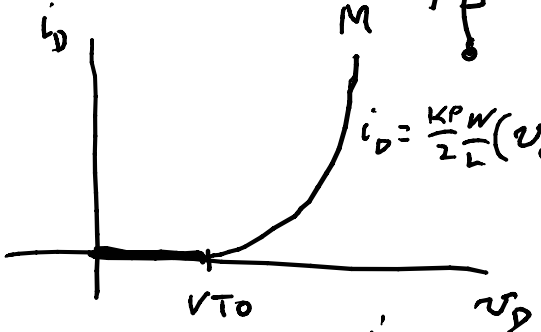
at the boundary $v_{DS} = v_{GS} - VTO$ (ohmic & sat)

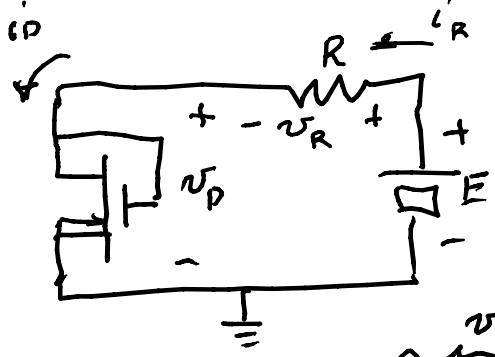
Diode connected

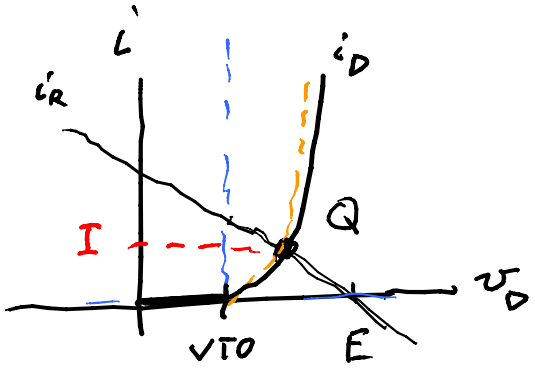
$v_{DS} = v_{GS} = v_D$

$\Rightarrow v_{DS} \ge v_{GS} - VTO$

$\Rightarrow$ M is in saturation if $v_{GS} - VTO > 0$ (otherwise in cut off)







KCL $i_R = i_D = \underbrace{G(E - v_D)}_{\text{Ohm's law}}$ v_R by KVL $\quad G = 1/R$

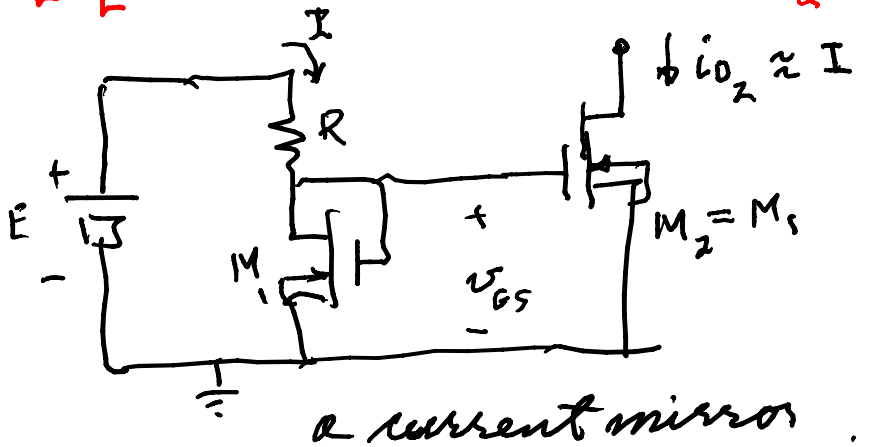
$= \frac{KP}{2}\frac{W}{L}(v_D - VTO)^2$

$x = v_D - VTO = VOD$

$= \beta_n x^2 = G(E - VTO - x) \Rightarrow$ quadratic in x

Given the transistor $I = \beta_n (v_D - VTO)^2 \Rightarrow v_{D_Q} = VTO + \sqrt{I/\beta_n}$

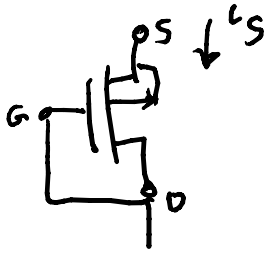
$\beta_n = \frac{KP}{2} \cdot \frac{W}{L}$ $\Rightarrow R = (E - v_{D_Q})/I$

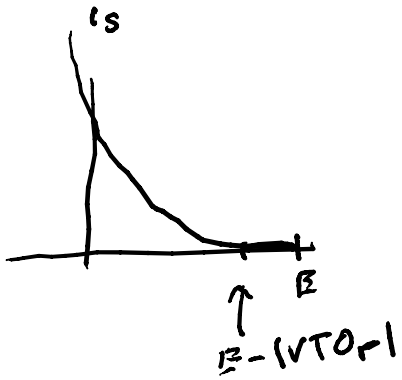


} v_{OS} be large enough to keep M_2 in saturation

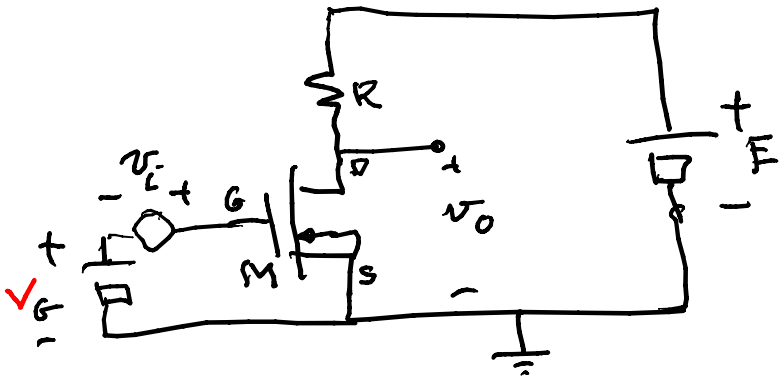
a current mirror

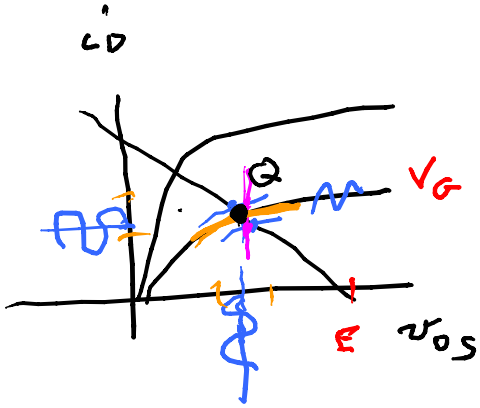
for R can use a PMOS





For amplification





assume Q is saturation point for M

$i_D = \beta (v_{GS} - VTO)^2 (1 + \lambda v_{DS})$

$V_{BS} = VTO$ when $v_{SB} = 0$

$i_D = I_D + i_d$

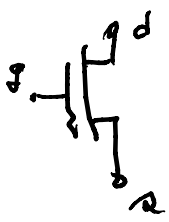
$x_y = X_y + x_y$

" " " total bias " signal

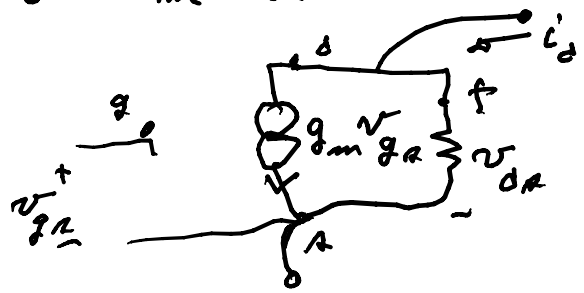
$i_D(v_{GS}, v_{DS}) = I_D + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q (v_{GS} - V_{GS}) + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q (v_{DS} - V_{DS}) + \text{higher orders}$

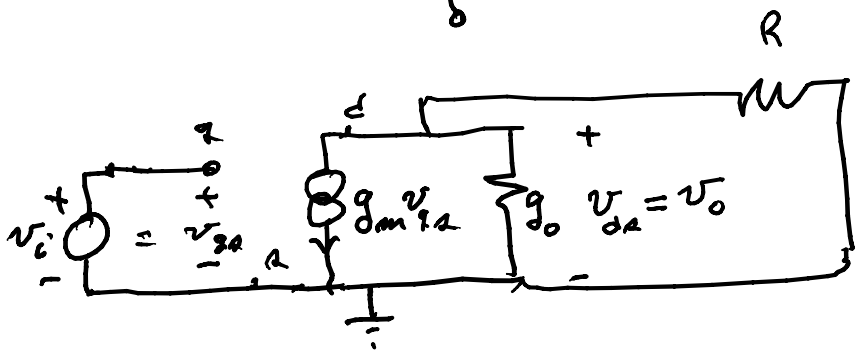
" $i_D(V_{GS}, V_{DS}) = I_{D_Q}$

$$\Rightarrow \quad i_d = i_D - I_D \simeq \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \frac{\partial i_D}{\partial v_{DS}} \cdot v_{ds}$$



$$i_d \simeq g_m \cdot v_{gs} + g_d v_{ds}$$





(low frequency [drop C_{gs}, C_{gd}]

$r_o = 1/g_o = 1/g_d$

of interest is $\frac{v_o}{v_i}$;

$$v_o = -(g_m v_{gs})\left(\frac{R r_o}{r_o + R}\right) = -g_m \cdot R_{L_{eq.}} \cdot v_i$$

$$\frac{v_o}{v_i} \simeq A_v = \text{voltage gain} \simeq -g_m \cdot R_{load}$$

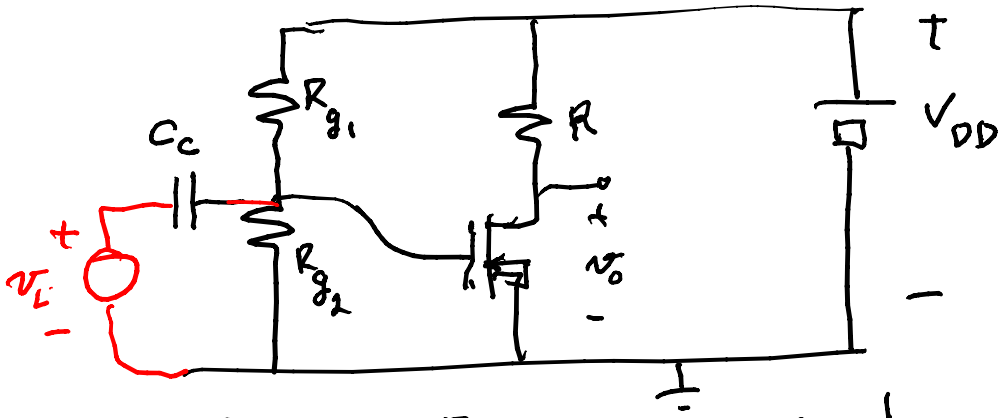
$$g_m: \quad \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = \beta \cdot 2 (v_{GS} - V_{TO})^2 (1 + \lambda v_{DS}) \Big| = \frac{2 I_D}{V_{OD}} \simeq 2\beta (V_{GS} - V_{TO})$$

$v_{GS} = V_{GS}$

$v_{DS} = V_{DS}$

$(v_{GS} - V_{TO})$

go to a voltage divides for the gate voltage



$$V_{GS} = \frac{R_{g_2}}{R_{g_1} + R_{g_2}} V_{DD}$$

$v_o / v_i \simeq -g_m R$

C_c = coupling capacitor (very large ea)

$$Z_c = \frac{1}{sC_c} \simeq \frac{1}{j\omega C_c}$$