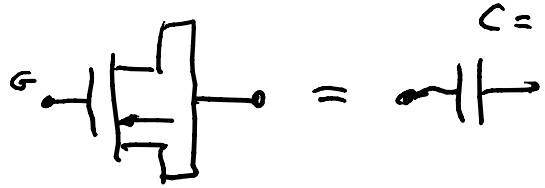
03/09/11
EE303

Note Title 3/9/2011

P. 704, Fig 9.5(a) & P. 706 Table 9.1 & P. 325 & eqn (5.107) (5.110, 5.111) = 4 terminal MOS small signal equivalent

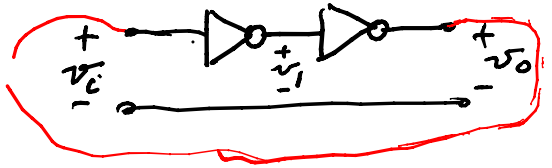
P. 1218, Fig. 15.12 = SRAM from inverters, P. 1205, Fig. 15.1



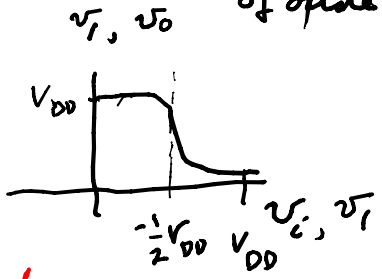
$C = W \times L \times C_{ox}$, $C_{ox} = \frac{\epsilon_{SiO_2}}{t_{ox}}$

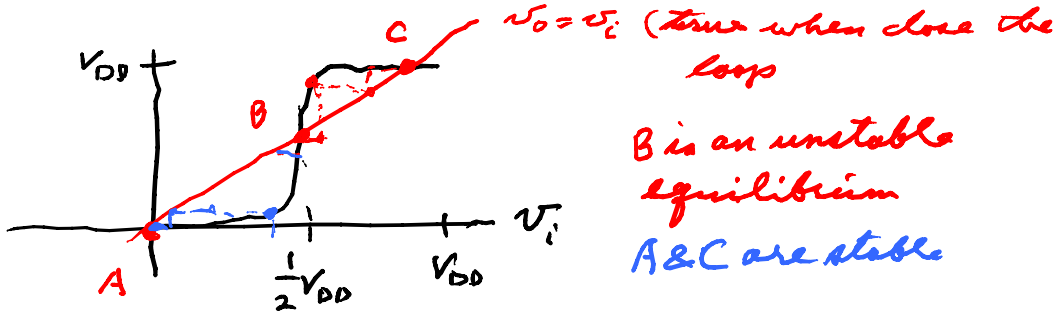
t_{ox} = thickness of oxide

Ring of 2 inverters



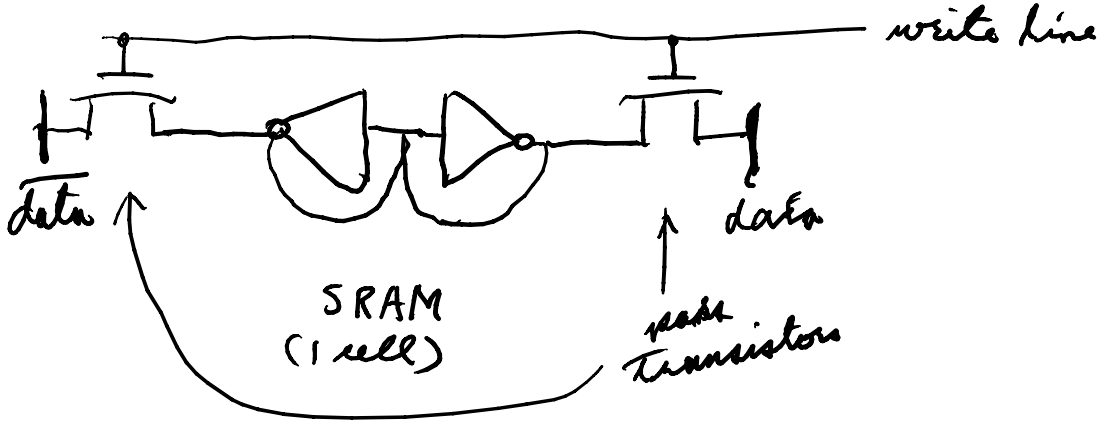
feedback



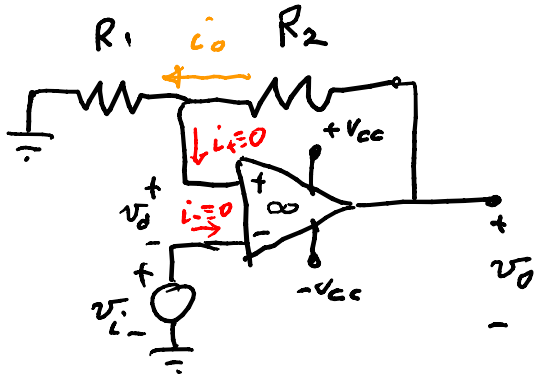


gives the SRAM = static random access memory

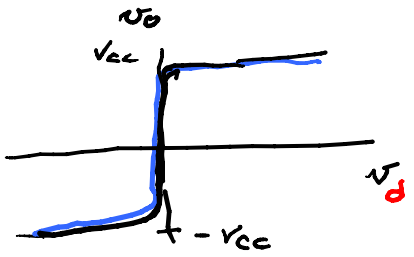
p. 1218 $\Rightarrow$ v_1 is complement of $v_o = v_i$



P. 1357, fig. 17.19 = Schmitt trigger



(can be a 4558 op. amp)
$\cong$ 1458



$v_o = R_2 i_0 + R_1 i_0 = R_2 i_0 + (v_d + v_i)$

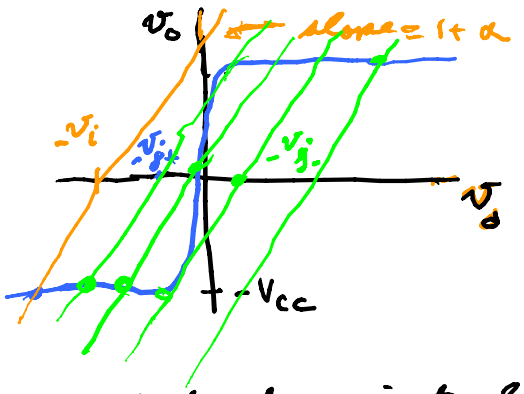
$\Rightarrow$ eliminate i_0 $\Rightarrow$ $i_0 = \frac{v_o}{R_1 + R_2}$ $\Rightarrow$ $v_o = R_2\left(\frac{v_o}{R_1+R_2}\right) + v_d + v_i$

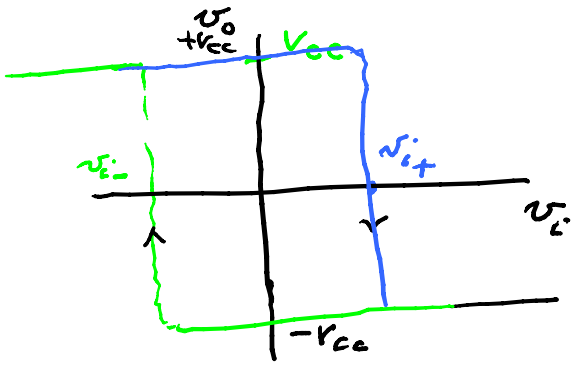
$\Rightarrow \left(1 - \frac{R_2}{R_1+R_2}\right) v_o = v_d + v_i$

$\alpha = \frac{R_2}{R_1}$

$\Rightarrow \left(\frac{1}{1+\frac{R_2}{R_1}}\right) v_o = v_d + v_i$

$\Rightarrow v_o = (1+\alpha) v_d + (1+\alpha) v_i$





To get break points desire when the line just hits V_{cc}

$$v_o = V_{cc} = (1+\alpha)\, v_d\Big| + (1+\alpha)\, v_i\Big| \quad \Rightarrow$$

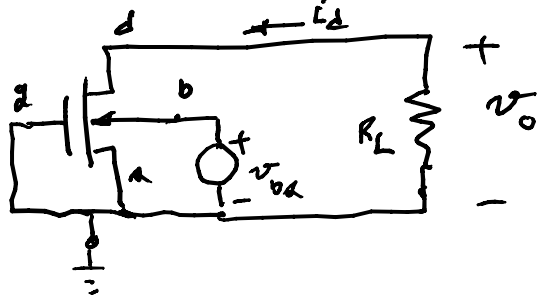
$v_d = 0$; v_i for jump down

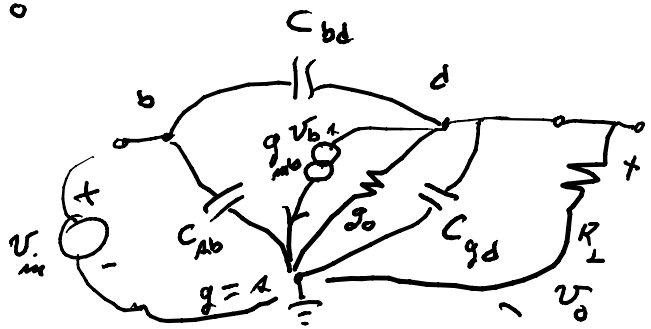
$$\Rightarrow v_i\Big|_{\text{jumps down}} = \frac{V_{cc}}{1+\frac{R_2}{R_1}} \quad = -\, v_i\Big|_{\text{jumps up}} = -\frac{V_{cc}}{1+R_2/R_1}$$

$$\text{hysteresis width} = v_i\Big|_{\text{jump up}} - v_i\Big|_{\text{jump down}} = \frac{2V_{cc}}{1+R_2/R_1}$$

gives design for hysteresis

Return to substrate as input see p. 720





$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}}$$

$$v_{th} = V_{TO} + \gamma\left(\sqrt{2\phi_s + V_{SB}} - \sqrt{2\phi_s}\right) \quad \text{eq. (5.107)}$$

$$i_D = \frac{KP}{2}\frac{W}{L}\left(v_{GS} - v_{th}\right)^2(1 + \lambda v_{DS})$$