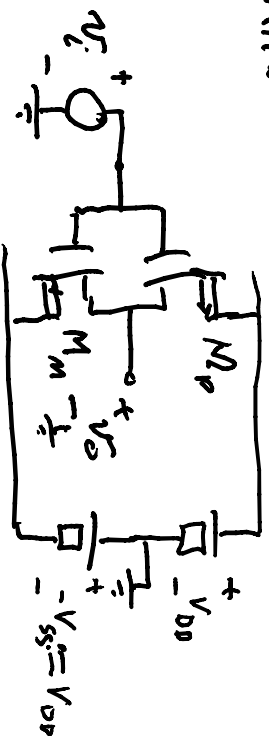


P. 1159 = pass transistor

P. 1359 = Schmitt trigger

P. 1119 = NAND

diodes



$$V_o = V_{OS} + V_{SS} \quad , \quad V_i = V_{GS} + V_{SS}$$

$$V_{OS} - V_{GS} = (V_o - V_{SS}) - (V_i - V_{SS}) = V_o - V_i$$

if  $V_{OS} - V_{GS} = 0$  then  $V_{OS} - V_{GS} = 0$

if enhancement mode  $\Rightarrow V_{OS} \geq V_{GS} - V_{TO_n}$

$$V_{TO_n} > 0 \Rightarrow V_{DS} > V_{GS} - V_{TO_n} \Rightarrow M_n \text{ is in saturation}$$

Also  $M_p$  is in saturation



but  $K_p < K_n$

As have to compensate by design of  $W_p$

$$\text{Then } I_{D_n} = I_{D_p} = -I_{D_p}$$

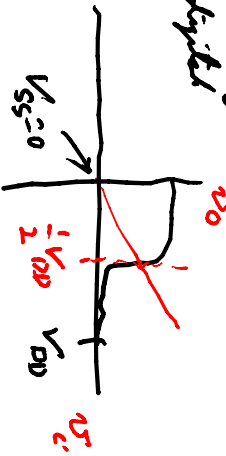
$$= \frac{K_n}{2} \left(\frac{W}{L}\right)_n (V_{GS_n} - V_{TO_n})^2 (1 + \lambda V_{DS}) = \frac{K_p}{2} \left(\frac{W}{L}\right)_p (-V_{GS} - V_{TO_n})^2 (1 + \lambda (-V_{DS}))$$

$$= \frac{K_p}{2} \left(\frac{W}{L}\right)_p (V_{SG_p} - V_{TO_p})^2 (1 + \lambda V_{SD}) = \frac{K_p}{2} \left(\frac{W}{L}\right)_p (V_{DD} - V_{TO_p})^2 (1 + \lambda V_{DD})$$

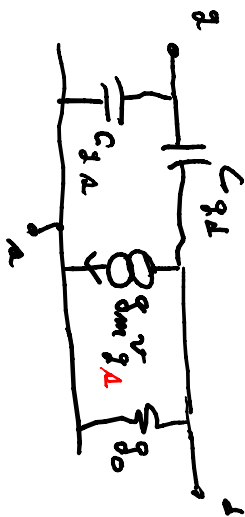
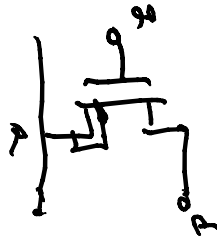
here solve for  $W_p$  if all else is known.

lines zero out for zero in.

on digital



Other MOS small signal:



$$Y = \begin{bmatrix} \lambda(C_{gs} + C_{gd}) & -\lambda C_{gd} \\ g_m - \lambda C_{gd} & \lambda C_{gd} + g_o \end{bmatrix}$$

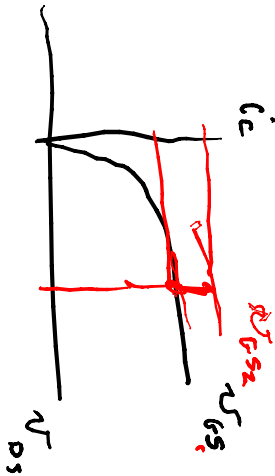
$$i_1 = i_g$$

$$i_2 = i_d$$

$$y_{11} = \frac{i_1}{v_1} \Big|_{v_2=0}$$

$$y_{21} = \frac{i_2}{v_1} \Big|_{v_2=0}$$

$$g_{dm} = \frac{\partial i_D}{\partial v_{gs}} \Big|_{v_{ds}}$$



$$i_D = \frac{k_p}{2} \left(\frac{W}{L}\right) (v_{gs} - V_{T0n})^2 (1 + \lambda v_{ds})$$

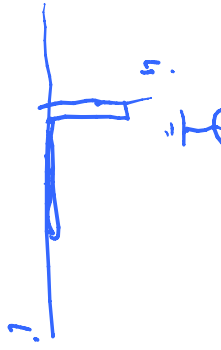
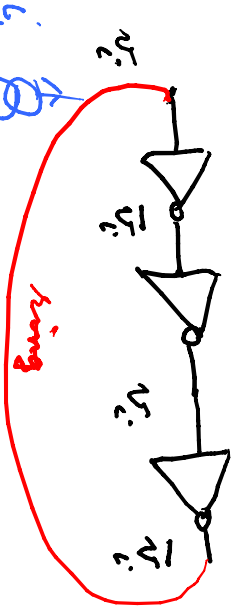
$$\frac{\partial i_D}{\partial v_{gs}} = 2 \frac{k_p}{2} \left(\frac{W}{L}\right) (v_{gs} - V_{T0n}) (1 + \lambda v_{ds}) = \frac{I_D}{(v_{gs} - V_{T0n})} = g_{dm}$$

# Ring oscillator

Symbol of inverter



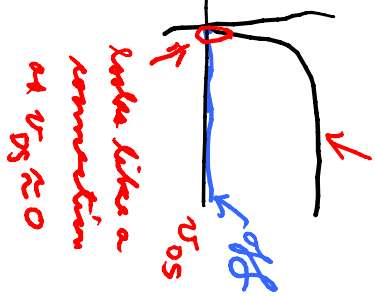
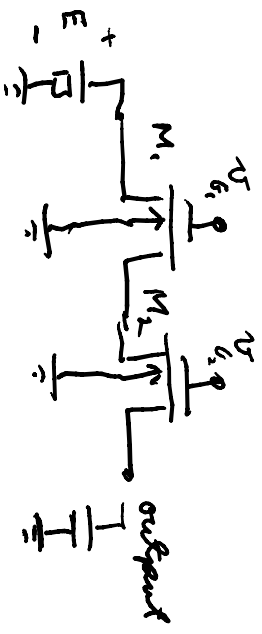
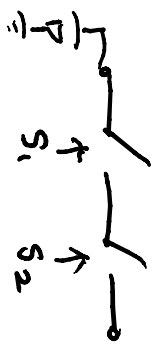
needs



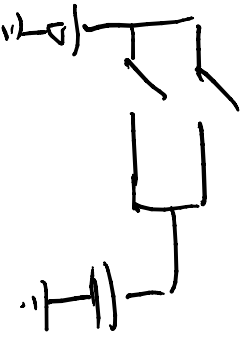
(switch level)  
one

## Pass transistors

and



both  $M_1$  &  $M_2$  are on when  $V_{G1} = V_{G2} = V_{DD}$



gives an  
or gate

implement a switch by putting N & P  
in parallel with complementary  
gate voltages.

Admittance inputs.