File: f:/coursesS11/303/303S11Hmwk5.doc RWN 03/06/11

ENEE 303 Spring 2011 – Homework 5 Due W 03/14/11

1. Simulate the two-input CMOS NAND gate of Figure 13.32 (page 1114, sixth edition)[=Figure 10.13, page 967, fifth edition] in PSpice using the 4007 transistors via the CA3600 part (in 14 pin package form) [this is in the Anl_misc library file]. Do this for the four possible digital logic input combinations [this can be done using two piece-wise linear (VPWL) input voltage sources]. Use the minimum possible number of packages and be sure to "tie off" unused transistors. Submit printouts containing the schematic and a plot having as sub-plots outputs and inputs. Run over enough time to compare the delay times for the different input combinations.

2. For the (all-pass) transfer function

$$\frac{vo}{vi}(s) = \frac{(s-5)(s^2-2s+6)}{(s+5)(s^2+2s+6)}$$

a) Give the (causal) impulse response (this can be done by making a partial fraction expansion and using the inverse Laplace transform; note that the behavior at infinity is not zero)

b) Give the sinusoidal steady state response to an input vi(t) = 2cos(3t).

3.Consider a CMOS inverter constructed with matched (complementary) transistors biased with a common gate voltage equal to Vdd=-Vss (all voltages with respect to ground and sufficient to adequately turn on the transistors). With such bias it can be used as an analog amplifier for which the admittance matrix is

$$Y = 2\begin{bmatrix} s(C_{gs}+C_{gd}) & -sC_{gd} \\ g_m - sC_{gd} & g_o + sC_{gd} \end{bmatrix}.$$

a) In terms of the Y matrix entries find the open-circuit voltage gain $\frac{vo}{vi}(s)$ and sketch the location of the zeroes and poles. .

b) If the transistors are 4007s give the resulting gm and go if Vdd=5V. Assuming Cgx =(WL/2)Cgxo with x = d or s, calculate Cgd and Cgs for these 4007 transistors.