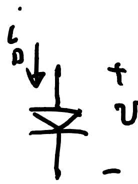
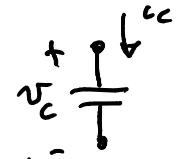
EE303
02/04/10

for next time
current sources/mirrors
MOS p. 563 & 649
BJT p. 442 & 650

differential pair
MOS p. 721
BJT p. 710



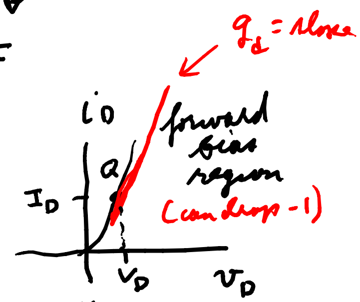
$$i_D = I_S\left(e^{v_D/V_T} - 1\right)$$

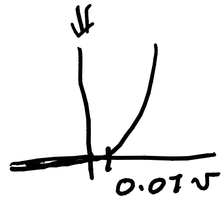


$$g_d = \left.\frac{\partial i_D}{\partial v_D}\right|_Q = \left.\frac{I_S e^{v_D/V_T}}{V_T}\right|_Q = \frac{I_S e^{V_D/V_T}}{V_T}$$

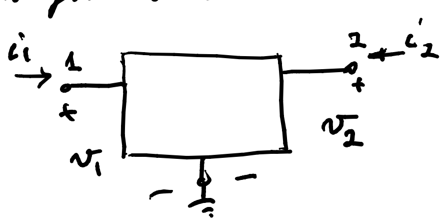
$$\approx \frac{I_D}{V_T} \text{ if forward biased}$$

$$r_d = \frac{1}{g_d} \approx \frac{V_T}{I_D} = \text{diode resistance}$$





Small signals ⇒ linear behavior



use admittance description; $Y(s)$ a 2x2 matrix

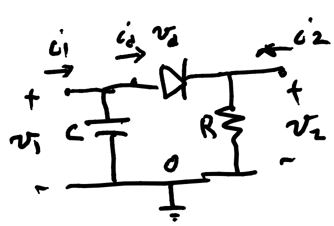
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = Y(s)\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

if $v_2 = 0 \Rightarrow i_1 = y_{11} v_1$
$i_2 = y_{21} v_1$

$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0}$ ⇒ short port 2

$y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0}$

Ex:



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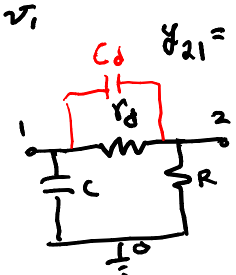
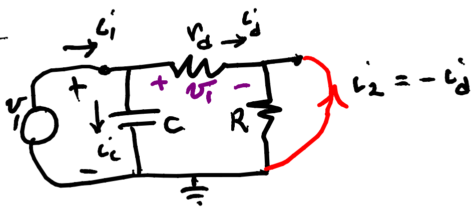
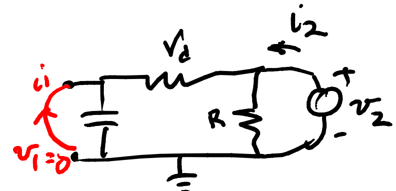


for y_{11} & y_{21} short port 2



$$y_{21} = \frac{i_2}{v_1}\Big|_{v_2=0} = -\frac{i_d}{v_1} = -g_d$$

$$y_{11} = \frac{i_1}{v_1}\Big|_{v_2=0} = \frac{i_d + i_c}{v_1} = +\frac{g_d \cdot v_1 + sCv_1}{v_1} = sC + g_d$$



$$y_{12} = \frac{i_1}{v_2}\Big|_{v_1=0} = -g_d$$

$$y_{22} = \frac{g_d \cdot v_2 + G v_2}{v_2} = g_d + G \qquad G = 1/R$$

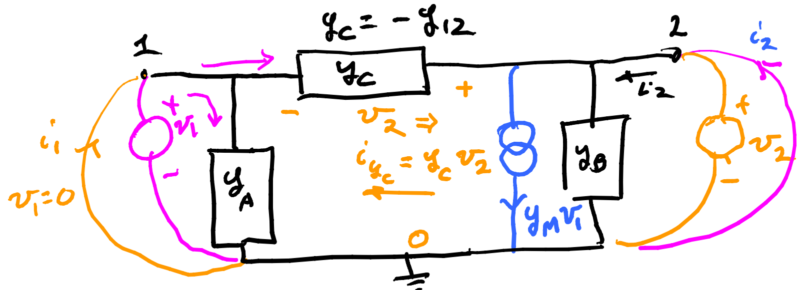
$$Y(s) = \begin{bmatrix} g_d + sC & -g_d \\ -g_d & g_d + G \end{bmatrix} \; ; \; Z = Y^{-1} = \frac{1}{g_d(sC+G)}\begin{bmatrix} g_d+G & +g_d \\ +g_d & g_d+sC \end{bmatrix}$$

$$= \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$$

note $z_{11} = \dfrac{g_d + G}{g_d(sC+G)}$

$$\neq \frac{1}{y_{11}} = \frac{1}{g_d + sC}$$

a universal equivalent circuit for $Y(s)$



$$y_{12} = \frac{i_1}{v_2}\Big|_{v_1=0} = -y_C$$

$$y_{11} = \frac{i_1}{v_1}\Big|_{v_2=0} = y_A + y_C$$

$$= \frac{y_C \cdot v_1}{v_1} + \frac{y_A \cdot v_1}{v_1}$$

— for $v_1 = 0$

— for $v_2 = 0$ node $2 = 0$

$$y_{21} = \frac{i_2}{v_1}\Big|_{v_2=0} = \frac{-y_C v_1}{v_1} + \frac{y_M v_1}{v_1} = y_{12} + \text{correction}$$

$$= -y_C + y_M$$

$$y_M = y_{21} + y_C = y_{21} - y_{12}$$

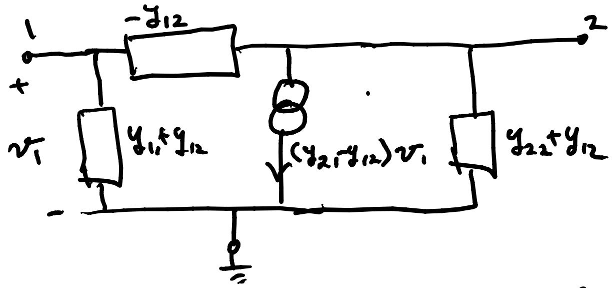
$$y_A = y_{11} - y_C = y_{11} + y_{12}$$

$$y_{22} = \frac{i_2}{v_2}\Big|_{v_1=0} = y_B + y_C$$

$$y_B = y_{22} - y_C$$

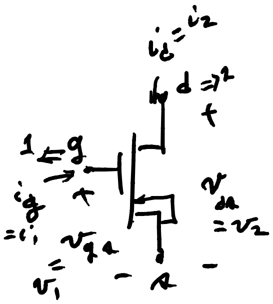
$$\therefore \quad = y_{22} + y_{12}$$

given $Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$



Π equivalent circuit

For the NMOS transistor small signal equivalent



at DC ; $i_1 = i_g = 0$

$i_d = g_m v_{gs} + g_d v_{ds}$

$i_2 = i_d$, $v_1 = v_{gs}$, $v_2 = v_{ds}$

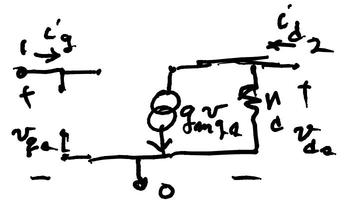
$\Rightarrow \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ g_m & g_d \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$

$g_d = \frac{I_D}{V_A} = \lambda I_D$

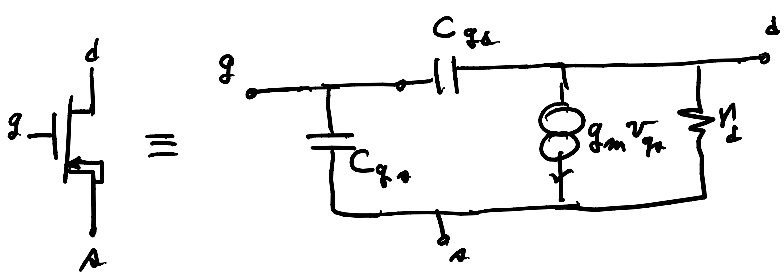
$g_m = \frac{I_D}{(V_{GS} - V_{TO})}$

in saturation region

$\Rightarrow$

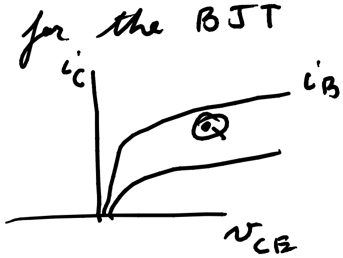


add in gate capacitors C_{gs} & C_{gd}

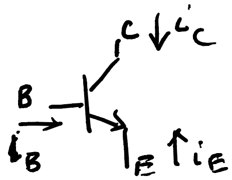


for "all"

for the BJT

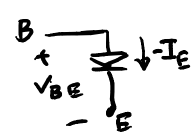


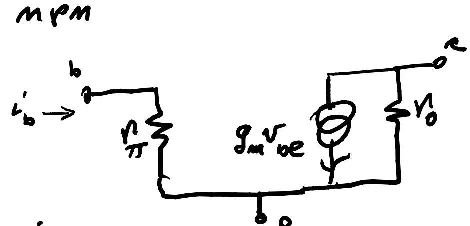
forward active



npn

for forward active region
diode CB we reverse bias
diode BE we forward bias





$i_B + i_C + i_E = 0$
by KCL
$i_C = -\alpha i_E$

$\left.\frac{\partial i_B}{\partial v_{BE}}\right|_Q = g_\pi = \frac{i_b}{v_{be}}$