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ENEE 303 Spring 2010 – Homework 6 Due Tu 04/06/10

1. Dram simulations
   For the dynamic RAM cell shown in Figure 11.21, page 1036, assume that the cell storage capacitance, Cs, is 50 pFarads, and the bit line capacitance, Cb, is 50 times larger. Assume that the transistor is an NMOS 4007 transistor and that all voltages mentioned below are with respect to ground, these being vb(t), vs(t) and vw(t) for the bit line voltage, the storage capacitor voltage and the word line voltage, respectively. Assume Vdd=5V and the precharge value of the voltage on Cb to be Vdd/2.
   a. Ignore transistor capacitors, the channel length modulation and the body effect. Set up the differential equation for the bit line capacitor voltage, vb(t). Do this for the initial storage capacitor voltage vs(0-)=Vdd and the word line voltage vw(t) being Vdd times the unit step function, 1(t). For this determine which terminal of the transistor is the drain and which the source and the region of operation of the transistor. Note that vs(t) can be eliminated since –Cs(dvs/dt)=Cb(dvb/dt) when the transistor is turned on. So first give the equation for vs(t) versus vb(t) for those t for which the transistor is turned on.
   b. Run Spice and check vs(t) & vb(t) and check against what you found in part b. for this use a VPULSE on the gate of the transistor with a small rise time and long pulse width and period or, alternately, a VPWL (where PWL= Piece-Wise Linear).
   c. Repeat parts a, b for the case of vs(0-)=0.