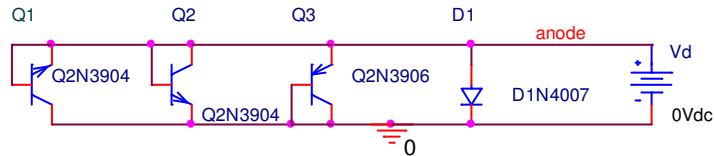
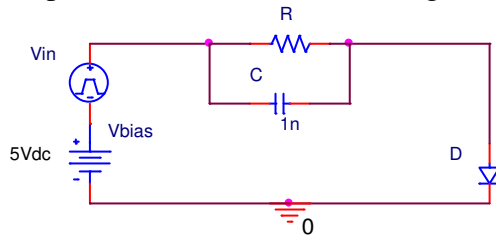


- Set up in Spice the following circuit and compare the diode curves. Plot in one “plot” the diode connected transistor diode characteristics and in another the 1N4007 diode’s. For this vary V_d from $-1.5V$ to $+0.85V$ and plot the diode currents (I_C for Q1, $-I_E$ for Q2, I_E for Q3). Also plot the full set of currents, I_B , I_E , and I_C for Q1, Q2, Q3, and compare.



- In the following circuit assume the diode is ideal in that it satisfies the exponential law, $i_D = I_S(\exp(v_D/V_T) - 1)$, but with the saturation current of the 1N4007, that is, $I_S = 14.1 \text{ nA}$. v_{in} is small signal, so assumed zero for setting bias.
 - Calculate the Q point V_D for $I_D = 3 \text{ mA}$ and with that the resistor value, R , needed for biasing (that is to give these V_D and I_D bias values).
 - Draw the small signal equivalent circuit assuming v_{in} is a small signal and set up the first order differential equation for the capacitor voltage.
 - From the small signal equivalent circuit find the small signal current (downward) in the diode when $v_{in}(t)$ is a unit step function of 1 microVolt amplitude (when the initial voltage on the capacitor is zero).



- In the above problem 2 circuit, with the diode a 1N4007, assume that R is a practical resistor with 5% tolerance. Do DC runs of Spice with the designed value of R (found in problem 2; also record the corresponding diode current I_D), then with R increased 5% and again with it 5% smaller. Show the resulting Q points in a printout of the diode with load line curves. Calculate the $\%$ change in I_D over that found with the designed value.
- Using the mnmosis and mpmosis transistors find the width of the mpmosis transistor needed to set the output voltage, V_o , of the following circuit to $3V$ (under no load conditions = open circuit where V_o is measured; note that both transistors are turned on and in the saturation region) include the Early effect.

