

ENEE 417 -Fall 2009

Week #5 starting M 02/23/09

Designs #2: Astable Multivibrator and Ring Oscillator Designs; VLSI & Spice Extraction

In this experiment a good reference is Sedra and Smith (pages 1026-1027 of the 5th edition)
For the active devices use the 4007 CMOS transistor package.

1. Construct the astable circuit of Figure 11-15 (a) of the above reference and make measurement to verify Figure 11.15(b) using various resistors and capacitors.
2. Construct both a three stage and a five stage ring oscillator and record via the GPIB the oscillations. Check the results of Figure 11.16 of the above reference.
3. Insert various capacitors at the outputs of the stages and see the effects. Among the capacitor values use one of the super-capacitors (whose values are on the order of Farads). Check also the effect of using an even number of stages.
4. In Spice use MOSIS 1.6u level 4 CMOS model parameters, available in the bicmos16.lib files, to design a three stage inverter (for this adjust the W and L so that a symmetric bias yields zero output voltage for zero input voltage; make sure that both W and L are bigger than 7microns). Based on your Spice design make a vlsi layout of your three stage ring oscillator. Using the layout obtain a Spice extraction. Insert the models used for your original Spice design and check that your layout gives comparable results to your original design.