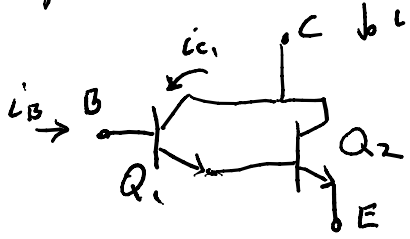
EE303
03/05/09

Darlington p. 645



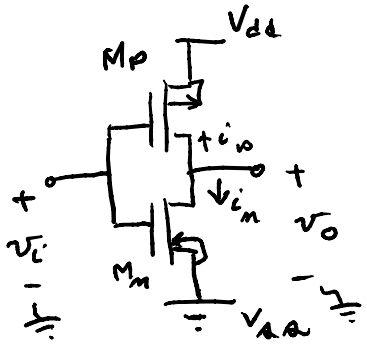
$i_C = \beta_1 i_B + \beta_2 i_{B_2}$; $i_{B_2} = -i_{E_1}$

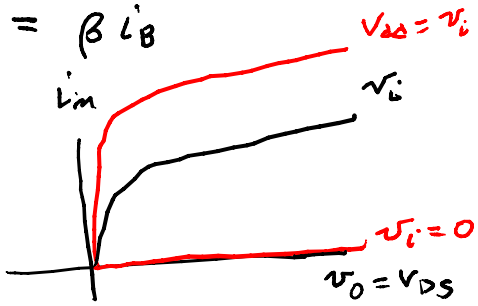
$= \frac{i_{C_1}}{\alpha_1} = \frac{\beta_1 i_B}{\alpha_1}$

$i_C = \left(\beta_1 + \frac{\beta_2 \beta_1}{\alpha_1}\right) i_B$

$= \beta i_B$

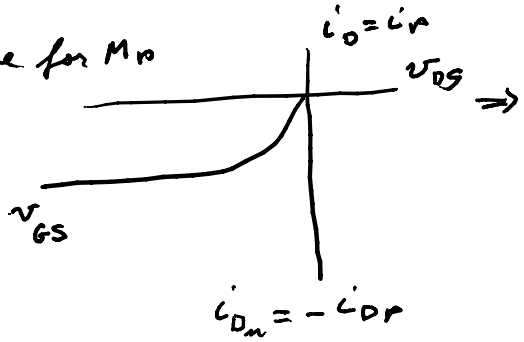
Load line & inverter CMOS



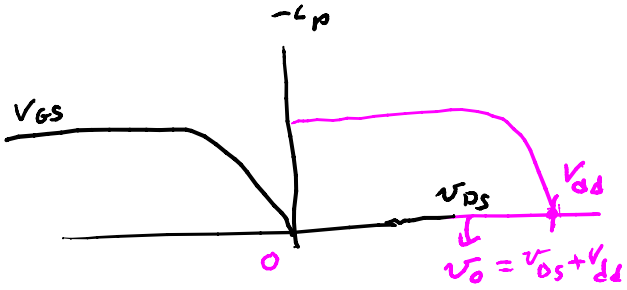


here $i_n = -i_p$; $v_{DS} = v_o - V_{dd}$

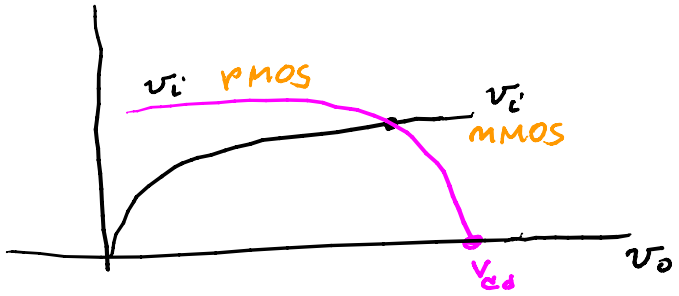
Curve for MP



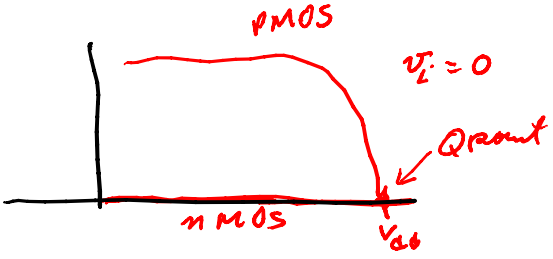
$\Rightarrow$

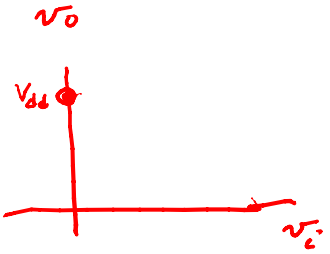


$i_{D_n} = -i_{D_P}$

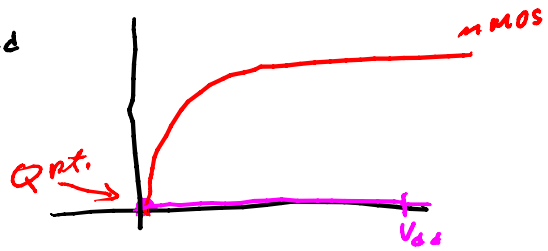


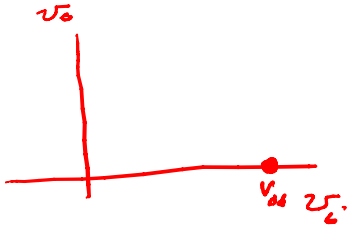
when $v_i = 0 = V_{dd}$



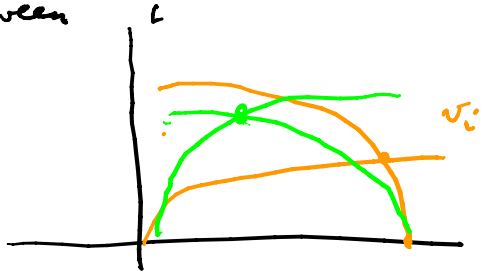


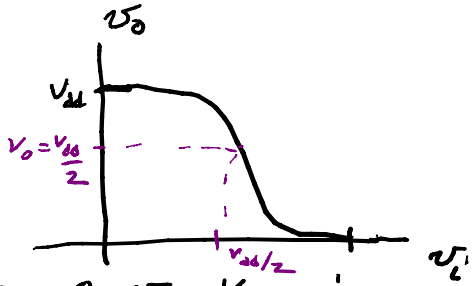
When $v_i = V_{dd}$





in between



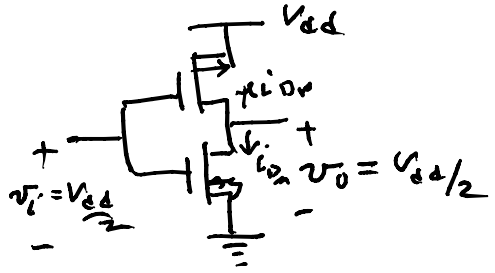


note no current is drawn at $v_i = 0$, $v_i = V_{dd}$

but in between there is. $\Rightarrow$ no power used except when transition

$\therefore$ useful for logics

How to achieve $v_o = V_{dd}/2$ when $v_i = V_{dd}/2$



$\Rightarrow V_{DS} = V_{GS}$

or $V_{DS} > V_{GS} - VTO$

$\Rightarrow$ implies saturation of NMOS & PMOS

to design:

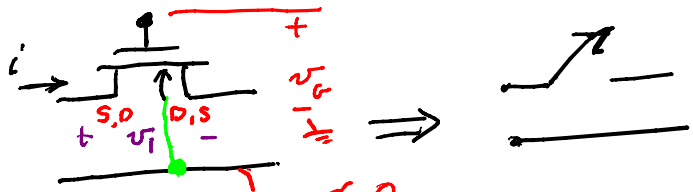
$$i_{D_n} = -i_{D_p} \Rightarrow \frac{KP_n}{2}\frac{W_n}{L_n}(v_{GS} - VTO_n)^2(1+\lambda_n v_{DS}) = \frac{KP_p}{2}\left(\frac{W}{L}\right)_p(v_{SG} + VTO_p)^2(1+\lambda_p v_{SD})$$

$$\Rightarrow \frac{KP_n}{2}\left(\frac{W}{L}\right)_n\left(\frac{V_{dd}}{2} - VTO_n\right)^2\left(1+\lambda_n \frac{V_{dd}}{2}\right) = \frac{KP_p}{2}\left(\frac{W}{L}\right)_p\left(V_{dd} - \frac{V_{dd}}{2} + VTO_p\right)^2\left(1 + \frac{\lambda_p}{\lambda_n}\left[V_{dd} - \frac{V_{dd}}{2}\right]\right)$$

for design we choose W/L 's; this is linear in their ratio

$$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n \cdot \left(\frac{KP_n}{KP_p}\right)\left(\frac{\frac{V_{dd}}{2} - VTO_n}{\frac{V_{dd}}{2} - |VTO|_p}\right)^2\left(\frac{1+\lambda_n V_{dd}/2}{1+\lambda_p V_{dd}/2}\right)$$

Pass transistor p.983



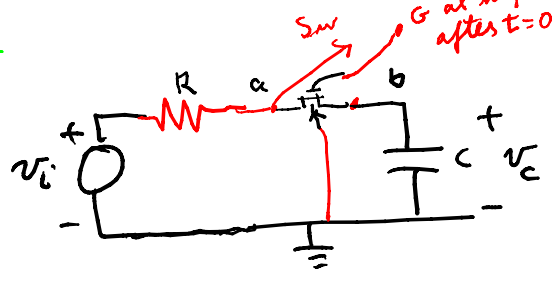
key points
Bulk should tie to V_{SS} to turn off the bulk to channel diode

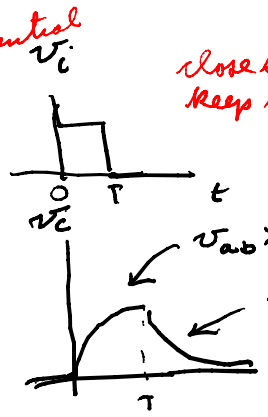
desire to be near the origin when we close the switch
dictate for V_{DS} to be most.
⇒ use $v_G = V_{dd}$ when turn on

want this small

at lowest potential ⇒ turns off the transistor

redone 03/06/09

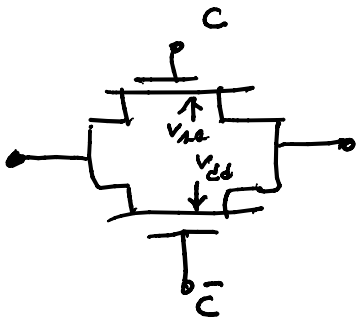




close switch at t = 0⁺ keep closed with V_{dd} on the gate

for Sw
$v_{ab} > 0$ ⇒ a = D rain, b = S ource
$v_{ab} < 0$ a = Source, b = Drain

Full "switch" has a CMOS pair

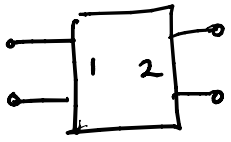


and & or gates
⇓ cascade
⇓ parallel

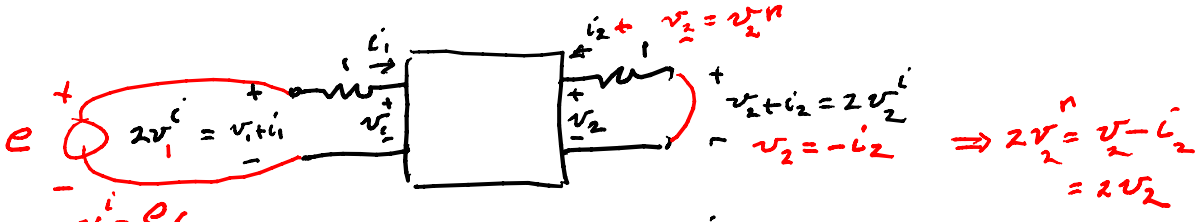
scattering matrix

$v^n = S v^i$

Y, $Z = Y^{-1}$, S

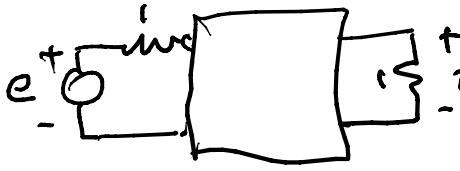


$2v^i = v + i$
$2v^n = v - i$
$v = v^i + v^n$
$i = v^i - v^n$



$$\begin{bmatrix} v_1^n \\ v_2^n \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} v_1^i \\ v_2^i \end{bmatrix}$$

$v_2 = 0$ $\quad v_2 = s_{21} v_1^i = \frac{s_{21}}{2} e$



$\Rightarrow s_{21}$ = voltage gain for a terminated 2-port

for $s_{11} \Rightarrow$ $v_1^n = s_{11} \cdot v_1^i$ when $v_2^i = 0$

$$v_1^n = \frac{v_1 - i_1}{2} = s_{11} \cdot \frac{e}{2}$$

$\Rightarrow s_{11}$ = reflection coefficient at the 1st port when terminate port 2 by 1 Ω.