1. NDR circuit

For the following negative differential resistor (NDR) circuit
a) Do a DC run and plot Iin vs Vin and calculate the maximum negative differential resistance (take Iin as up through Vin so it is the current flowing into the NDR).
b) Vary Wn and then Wp and note the differences

2. Use this NDR Iin vs Vin as the $\mathrm{F}(\mathrm{Vin})$ for realizing by a CMOS-C circuit the oscillator state variable equations

$$
\begin{aligned}
& \frac{\mathrm{dx}_{1}}{\mathrm{dt}}=\mathrm{x}_{2}-\mathrm{F}\left(\mathrm{x}_{1}\right) \\
& \frac{\mathrm{dx}{ }_{2}}{\mathrm{dt}}=-\omega_{\mathrm{o}}^{2} \mathrm{x}_{1}
\end{aligned}
$$

a) Set this up in Spice; use $\omega_{0}=1$ (justified by time-capacitor normalization)
b) Show via Spice transient analysis, plotting $x_{2}(t)$ vs $x_{1}(t)$, that there is a limit cycle.
c) Plot the Spice time functions $\mathrm{x}_{1}(\mathrm{t})$ and $\mathrm{x}_{2}(\mathrm{t})$ for the limit cycle.
3. Repeat problem 1 for the following double NDR circuit and investigate obtaining two limit cycles using the equations of 2 . Note that the right portion is a copy of the circuit in problem 1 but with a diode connected NMOS which forces the PMOS to turn on at a larger Vin to give the second valley.


