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Homework Set 5 due ~~Friday 03/02/07~~ Monday 03/05/07

For these problems use the Spice model parameters for the 4007 CMOS transistors, these being nch and pch in the CA3600E part in the Anl_misc libraries.

1. [50 points] (CMOS inverter)

For the CMOS inverter, the "final" two as they are already connected in the 4007 package (gates connected to pin 10 and drains to pin 12) [the same as Fig. 10.4(a), p. 956, except with the ground replaced by V_{SS}]:

a) Assume $V_{DD} = -V_{SS}=5V$ and the input (=gate) voltage of 0V, calculate the output voltage, Vo, (be sure to include LAMBDA).
b) Assume $V_{DD}=5V$, and the input voltage of 0Vand that the Early effect is negligible (that is LAMBDA can be ignored), calculate V_{SS} to give Vo = 0.
c) Taking into account the Early effect repeat part b) [note this requires solving a cubic equation which you can do by some numerical analysis program, though exact formulas exist].
d) Check as much of the above as possible via Spice runs.

2. [50 points] (CMOS gates)

By using the CA3600E Spice transistor package, simulate the nand gate circuit of Figure 10.13, p. 967. For this use $V_{DD} = 5V$ and pulses which have pulse widths of 1millisec (and very small rise and fall times); verify all entries in the nand truth table. Submit the package connections (via a PSpice schematic printout) used along with appropriate transient response curves indicating how they verify the truth table entries. Note that you can do this by using the Spice piece-wise linear voltage sources VPWL.