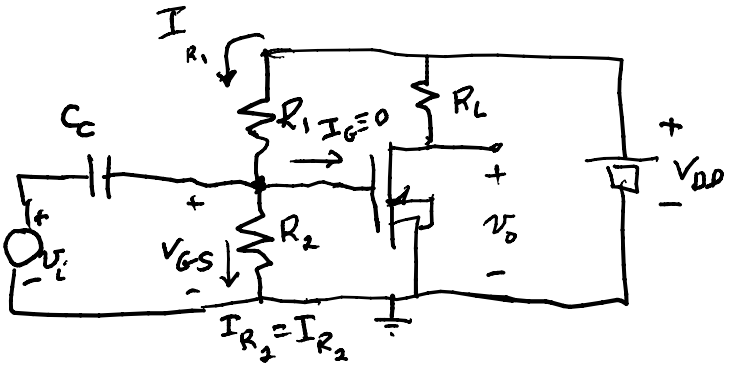
EE 303
02/19/07



$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

$$V_{GS} = R_2 I_{R_2} = \frac{R_2}{R_1 + R_2} V_{DD}$$

(voltage divider)

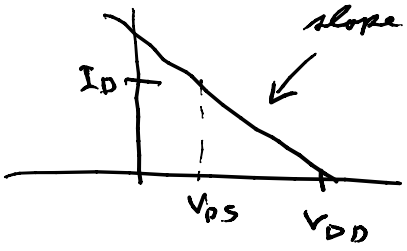
C_c = coupling capacitor

$Z_{C_c} = \frac{1}{AC}$ at DC (bias) $s \to 0$ or C_c opens up for bias

input on left sees R_1 & R_2 in parallel; if small R_{11} this puts a load on the input circuit on the left

note $V_{GS} = \left(\frac{1}{1 + \frac{R_1}{R_2}}\right) V_{DD}$ so can make R_1 & R_2 large (use in MEG Ohm range)

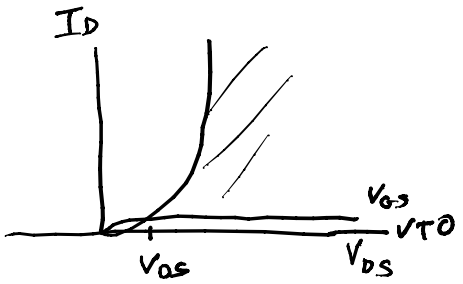
How to adjust the gain: $|\text{Gain}| = g_m / G_L = \dfrac{\frac{2 I_D}{V_{GS} - VTO}}{\frac{-I_D}{V_{DS} - V_{DD}}}$



$\text{slope} = -G_L = \dfrac{I_D - 0}{V_{DS} - V_{DD}}$

$= 2\left(\dfrac{V_{DD} - V_{DS}}{V_{GS} - VTO}\right)$ where $V_{DS} > V_{GS} - VTO$ (sat)

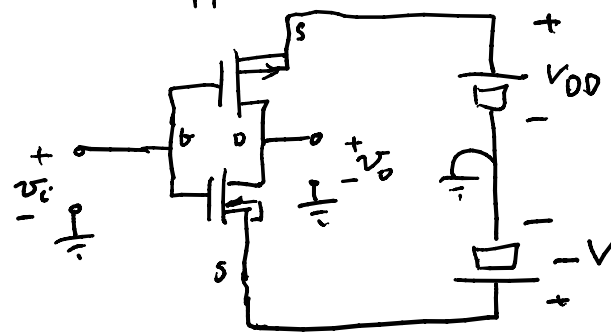
(can get close to ∞ gain by $V_{DS} \to 0$ & $V_{GS} \to VTO$ but decreases linearity region)



Inverter – CMOS

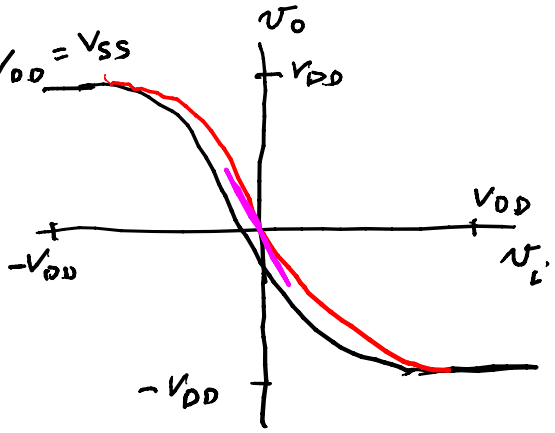
"complementary (N&P)

PMOS



NMOS

Must bias by choice of P & N to get $v_o = 0$ when $v_i = 0$



desire $v_o = 0$ when $v_i = 0$

$V_{GS}\big|_{\substack{v_i=0 \\ PMOS}} = -V_{SG}$, $V_{SG} = V_{DD}$; $V_{SD} = V_{DD}$

$V_{GS}\big|_{NMOS} = V_{DD}$; $V_{DS} = +V_{DD}$; $V_{DS} \quad V_{GS} - VTO = V_{DD} - VTO$

$V_{DD} > V_{DD} - VTO \Rightarrow$ NMOS is in saturation

$\Rightarrow$ PMOS also in saturation.

$$V_{SD_p} = V_{DD} > V_{SG_p} - (-VTO_p) = V_{DD} - |VTO_p|$$

$$V_{DS_p} < V_{GS_p} - VTO_p$$

$$-I_{D_p} = I_{D_n}, \quad I_{D_n} = \frac{KP_n}{2}\left(\frac{W}{L}\right)_n (V_{GS} - VTO_n)^2 (1 + \lambda_n V_{DS}) \qquad (V_{GS} = V_{DD},\ V_{DS} = V_{DD})$$

$$-I_{D_p} = \frac{KP_p}{2}\left(\frac{W}{L}\right)_p \left(V_{SG_p} - |VTO_p|\right)^2 (1 + \lambda_p V_{SD_p}) \qquad (V_{SG_p} = V_{DD},\ V_{SD_p} = V_{DD})$$

here can find $\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n \left(\frac{KP_n}{KP_p}\right)\left\{\frac{(V_{DD} - VTO_n)^2 (1 + \lambda_n V_{DD})}{(V_{DD} - |VTO|_p)^2 (1 + \lambda_p V_{DD})}\right\}$

allows $v_0 = 0$ when $v_i = 0$.