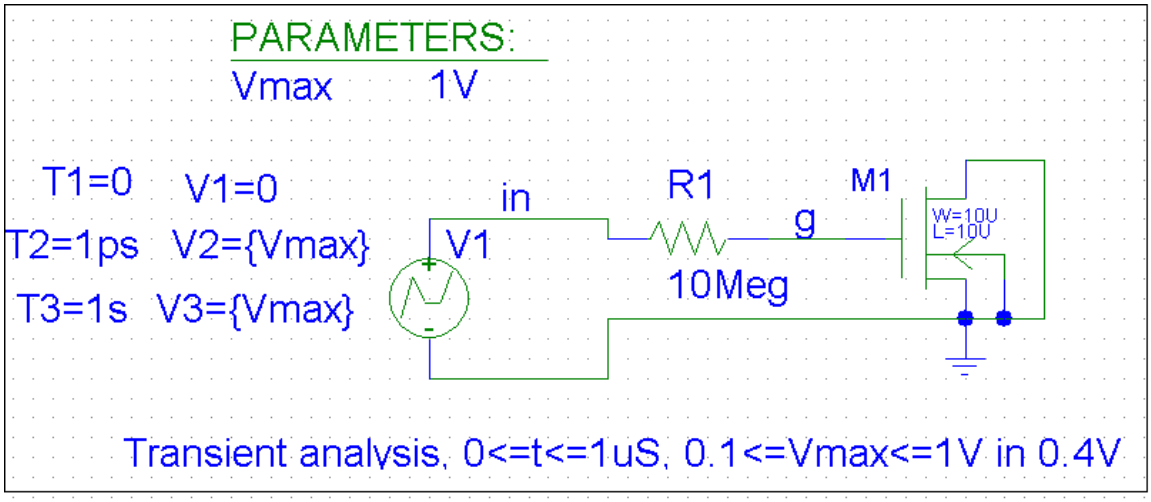
File: E:/courses/spring2006/303/hmwrk4.doc RWN 02/22/06

Homework Set 4 due Wednesday February 29, 2006

1. [50 points]
   Design three types of vlsi capacitors using the 2.0u AMI technology with all devices being 10u by 10u (that is, W=10u, L=10u). The data for these is (found from the MOSIS web page):
   Oxide Thicknesses:
   metal 2 to metal 1: 6,500 Angstroms
   poly 2 to poly 1: 760 Anstroms
   poly 1 gate oxide: 400 Angstroms
   (use dielectric=SiO2, see p. 243 of text for epsilon_ox)
   For MOS transistors assume that the gate capacitances are modeled as per section 4.8 (p. 320+) of the text.

A. Give the values of capacitance and compare for the following cases.
   a) Using poly 2 over poly 1
   b) Using metal 2 over metal 1
   c) Using an NMOS with B, D, & S tied together with C between G&S.
   d) Using a PMOS with B, D, & S tied together with C between G&S.

B. Using Spice plot Vout versus time for the following circuit for each case of the above capacitors used at the right of the following circuit (replacing M1 for all but the NMOS C). Also plot all transistor currents and discuss why some are zero and others not.



2. [40 points]
   For the BN2X4 transistors draw the pi equivalent circuit when biased at IC=2uA and find the DC voltage gain when loaded by 10KOhm and fed from a voltage source of 50 Ohm source resistance. Assuming $C_{\rightarrow}$=3pFd and $C_{\blacktriangleright}$=1.5pFd, find the voltage transfer function Ta(s)=vout/vin.

3. [10 points]
   Rework problem 2 of homework set 2.