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Homework Set 3 due Wednesday February 22, 2006

1. [50 points]

For an NMOS transistor in the Ohmic region, with the bulk tied to the source, use the DC description

$$i_D = \frac{KP}{2}\frac{W}{L}[2(v_{GS} - VTO)v_{DS} - v_{DS}^2](1+\lambda v_{DS})$$

a) find analytic expressions for g_m and g_o

b) using KP=4*10E-5 A/V^2,W=3L=10microns, VTO=0.6V, λ=lambda=0.01/V, evaluate i_D, g_m, and $r_o = 1/g_o$ at the bias point V_{GS}=2V, V_{DS}=0.5V

c) draw the small signal equivalent circuit including the non-DC components Cgs=3Cgd/2=3pFd.

d) find the voltage transfer function, Vout(s)/Vin(s) for an input applied to the gate (with respect to ground) and the output across a 10KOhm load at the drain (with respect to ground).

2. [50 points]

Using 4007 MOS transistors design the following current mirrors to mirror an input current of 2mA for a desired output current of 2mA. In all cases give the Spice circuit and output current versus output voltage (that at the drain of the output transistor) for 9V≥Vout≥0. Discuss differences in the results and the amount of hardware needed.

a) A basic current (sink) mirror of Figure 6.5, p. 563.

b) A basic current (source) mirror as on the right of Figure 6.7, p. 566.

c) The modified Wilson mirror of Figure 6.61(c).

3. [50 points]

For the npn BN2X4 transistors of the 2.0u technology MOSIS set:

a) give Spice plots for i_C versus v_{CE} with i_B as a parameter with $5V \geq v_{CE} \geq 0$ for $9uA \geq i_B \geq 0$ in 3uA steps.

b) draw the small signal equivalent circuit for this transistor when biased at I_C = 0.46mA, I_B = 6uA. Also give theV_{CE} for this bias point and indicate the Q point on the Spice curves. .