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Homework Set 2 due Wednesday February 15, 2006

1. [50 points]

An MOS transistor in the saturation region is described for DC by the equations

$$i_D = \frac{KP}{2}\frac{W}{L}(v_{GS} - Vth)^2(1 + \lambda v_{DS})$$

$$Vth = VTO(1 + \frac{v_{BS}}{VT}) \quad = \text{threshold voltage (as a function of bulk to source voltage)}$$

with constants KP=4*10E-5 A/V^2,W=3L=10microns, VTO=0.6V, λ=lambda=1/VA, VT=thermal voltage=0.026V, VA=Early voltage=100V. For non-DC behavior assume Cgs=3Cgd/2=3pFd, p=pico=10E-12.

a) When biased at V_{BS}=0, V_{GS}=2v, I_D=2ma give the value of V_{DS} and draw the small signal equivalent circuit indicating the component names and their numerical values.

b) Check if the transistor is actually biased in the saturation region. Assuming V_{GS} fixed find the value of I_D, and with it V_{DS}, at which the transistor transitions from the Ohmic region to saturation.

c) Assume that the bulk to source current is given by the diode law

$$i_{BS} = IS(e^{v_{BS}/VT} - 1)$$

With IS=2pAmp, and the bulk to source bias changed from that in part a) to V_{BS}=0.5V, insert a bulk terminal in the small signal equivalent circuit and give the value of the inserted component(s).

2. {50 points]

Using a 4007 NMOS transistor design a common source amplifier to give a small signal (open circuit loaded) voltage gain of 10 at an output bias voltage of 2.5V=Vdd/2. For this draw the full circuit, describe how you biased the transistor (including the gate and bulk), draw the small signal equivalent circuit and the equations used to make the design (both bias and small signal portions)[evaluate using the Spice parameters for the 4007 transistor].