EE303
03/17/06

CMOS gates

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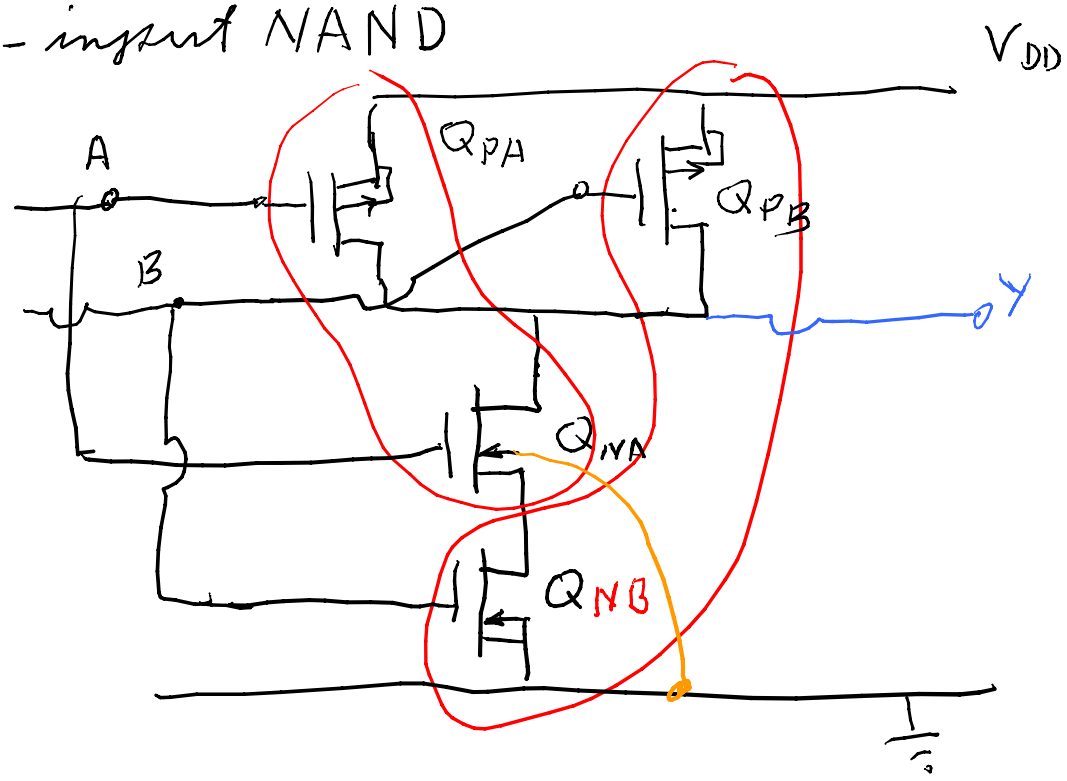
2-input NAND



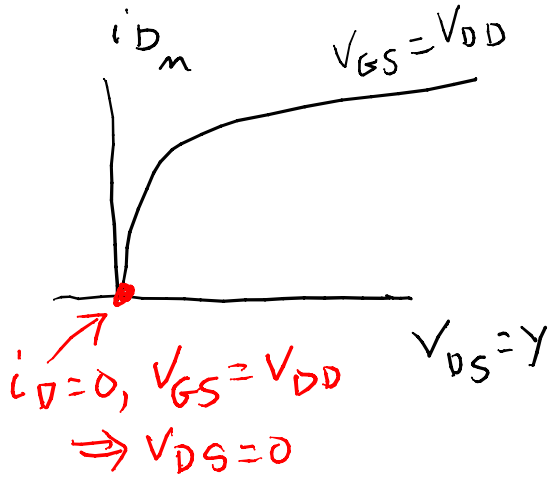
if A=0, Y=1 (no matter B

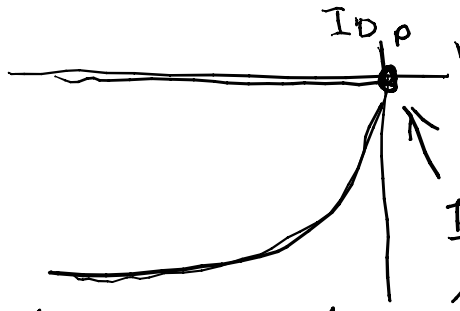
B=0, Y=1 (no matter A

A & B=0, Y=1

A & B=1, Y=0

when A & B=1





when A or B = 0

$-V_{GS} = V_{SG} = V_{DD}$ $\Rightarrow V_{DS} = 0 \Rightarrow Y = V_{DD} - V_{SD}$

$= V_{DD}$

note substrate on Q_{NA} is not tied to the source unless put in a separate P-well if made on one chip. Means that $V_{th_{NA}} \neq VTO_n$

$$V_{th} = VTO + GAMMA\left(\sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f}\right)$$

Eq. (4.33)

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