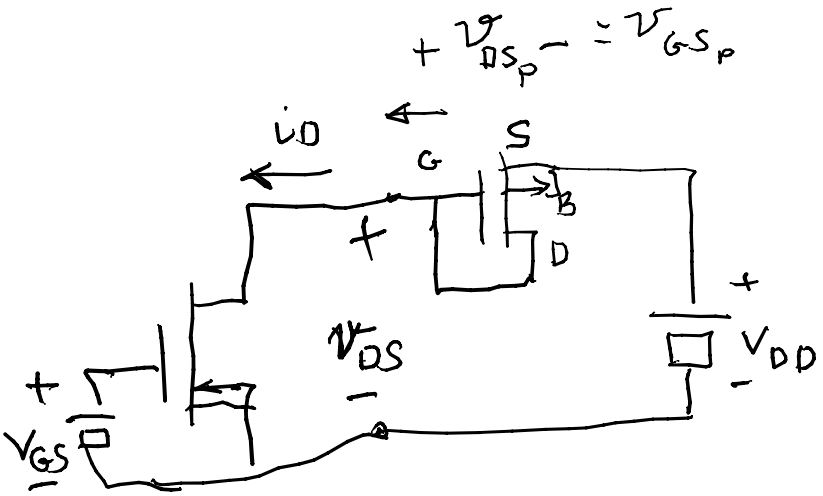
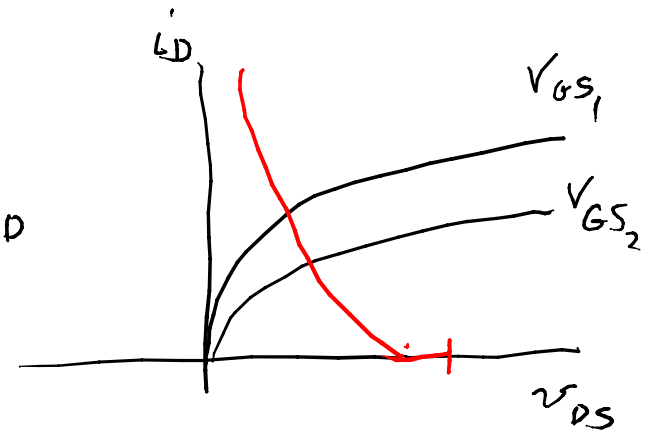
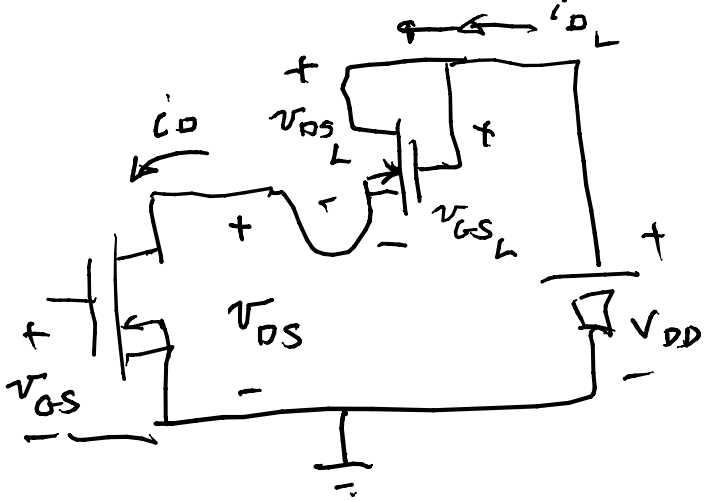
EE303
02/13/06



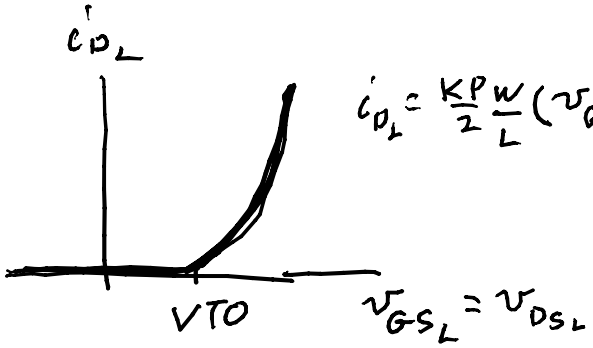




$v_{GS_L} = v_{DS_L}$ in sat if

$0 \le v_{GS_L} - VTO \le v_{DS_L}$

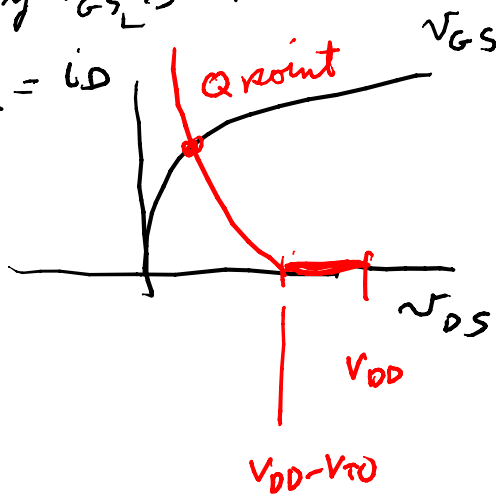
if on — true if $v_{GS_L} = v_{DS_L}$

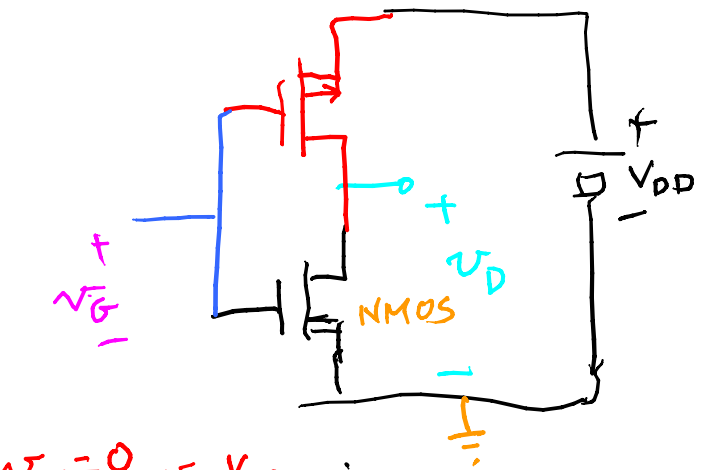


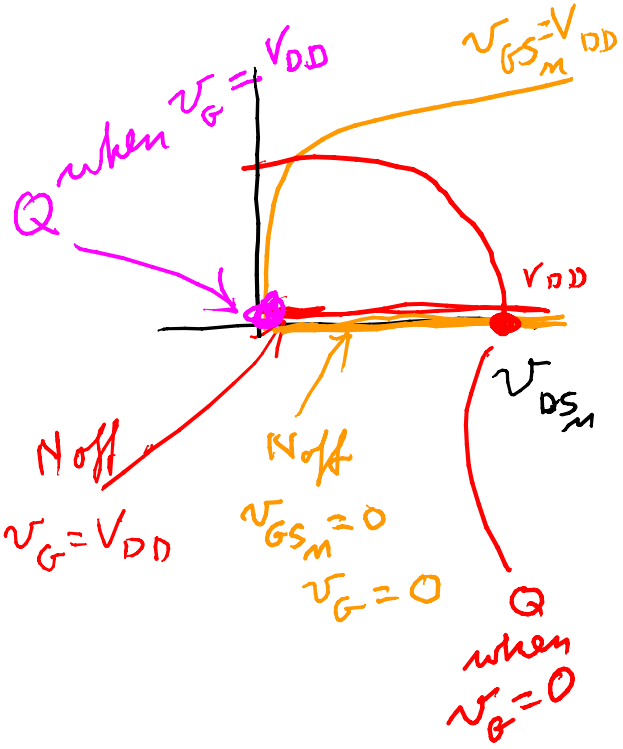
$i_{D_L} = \frac{KP}{2}\frac{W}{L}(v_{GS_L} - VTO)^2$ if $v_{GS_L} \ge VTO$

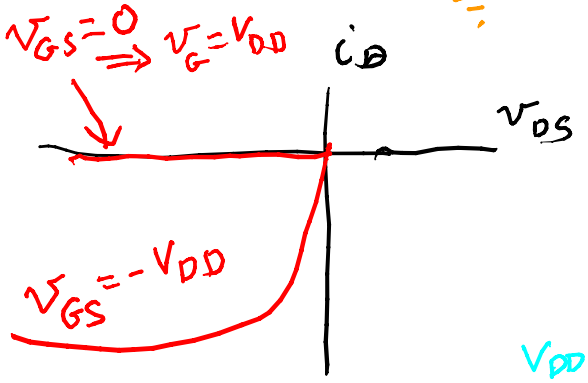
$i_{D_L} = i_D$

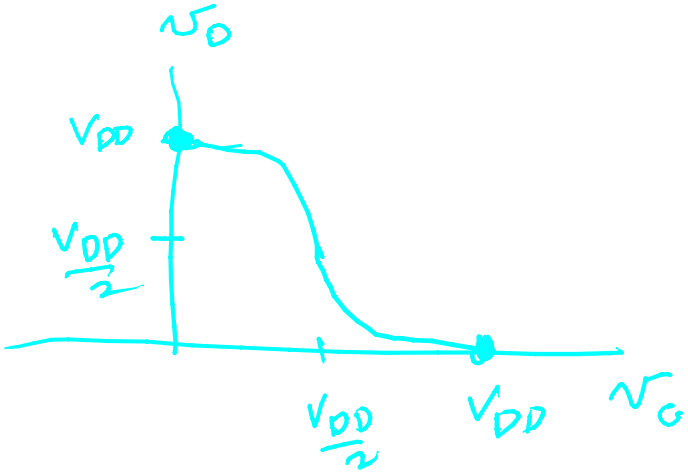
$v_{DS} = V_{DD} - v_{DS_L}$



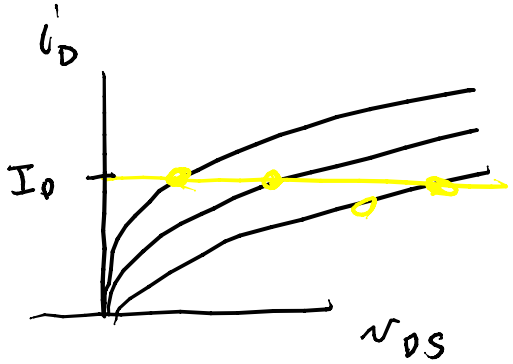




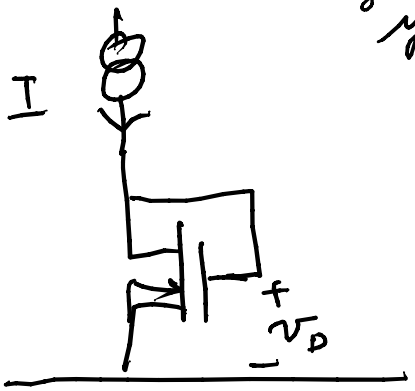


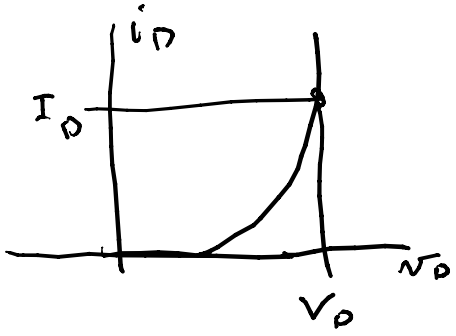


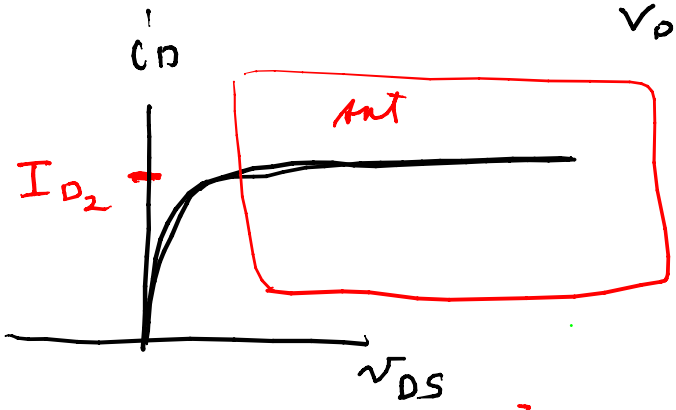
Current Mirror



connect D–G gives a single valued v vs i
if a diode connected MOS is on

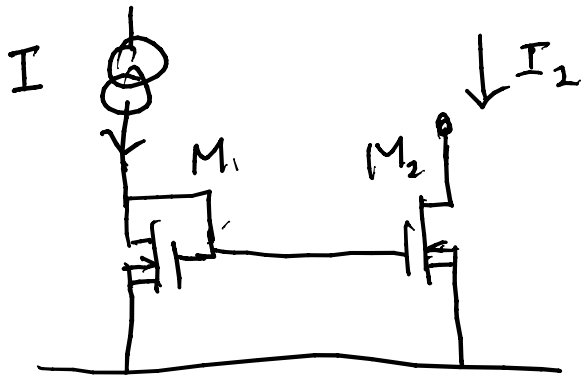






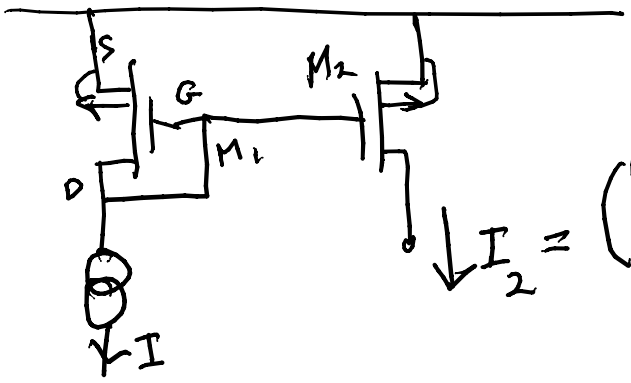
$$I_{D_2} = \frac{KP}{2}\frac{W}{L}(V_{GS} - VTO)^2$$

if stay in saturation on M_2 then I_2 mirrors the first



$$\downarrow I_2 = \left(\frac{(W/L)_2}{(W/L)_1}\right) I_1$$

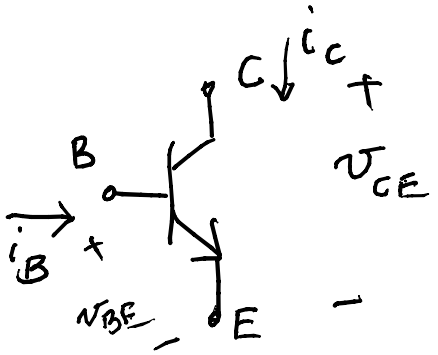
a current sink (mirror)

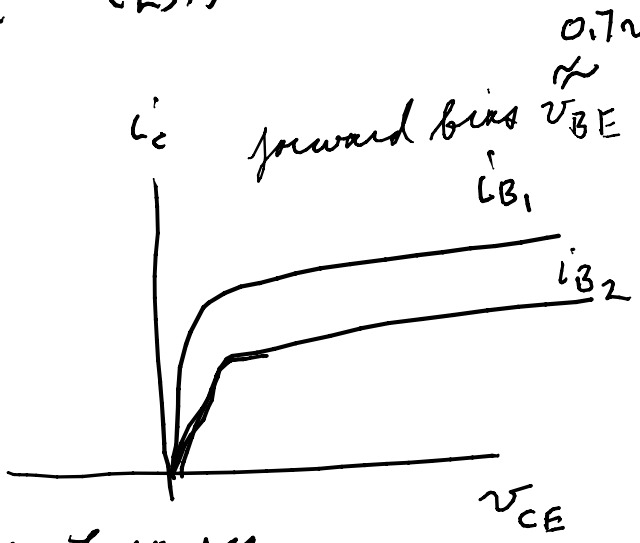


$$I_2 = \left(\frac{(W/L)_2}{(W/L)_1}\right) I$$

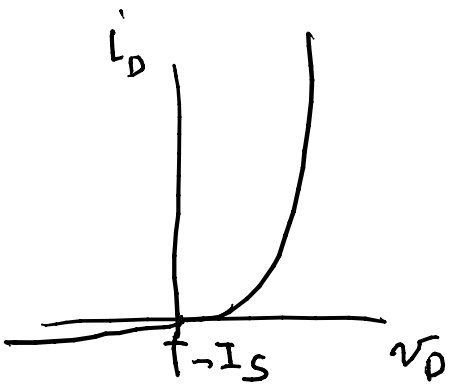
a source mirror

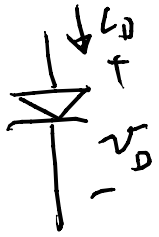
BJT



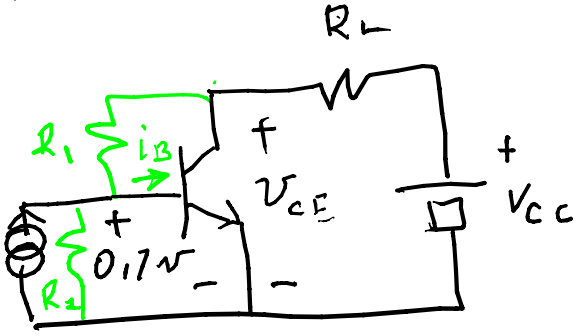


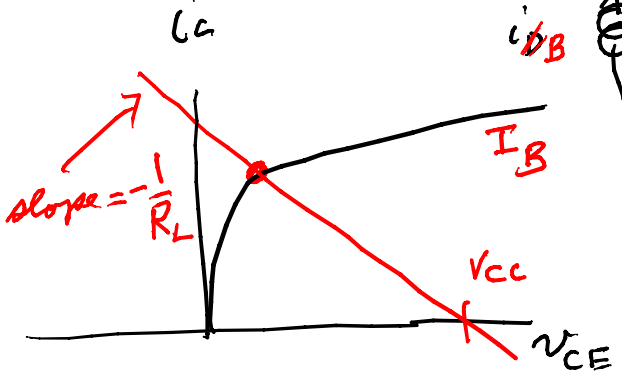
current controlled current source





$$i_D \simeq I_S\left(e^{v_D/V_T} - 1\right)$$





$i_B \neq 0$ so R_1 & R_2 not quite a voltage divider $\Rightarrow$ R_2 has $0.7V$ DC on it and $I_B + I_{R_2}$ flows in R_1 for biasing