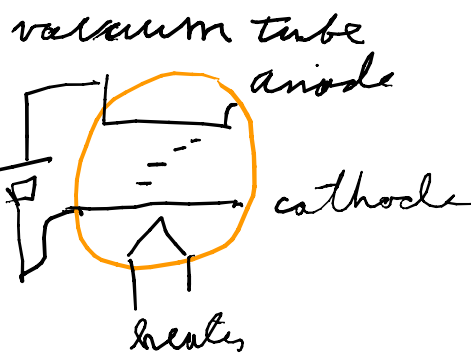
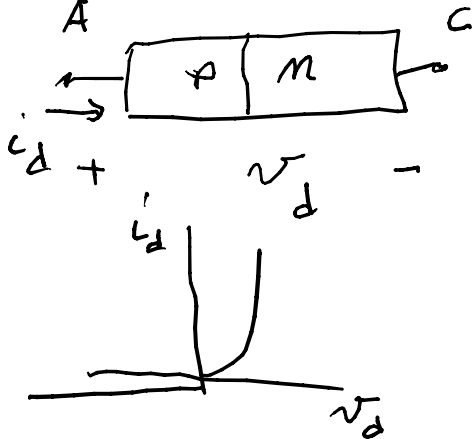


EE 303
01/27/06

junction diode



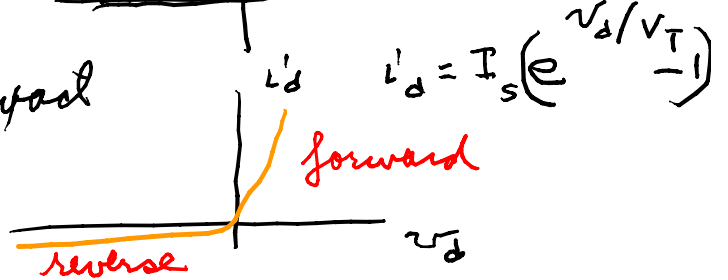
ideal model



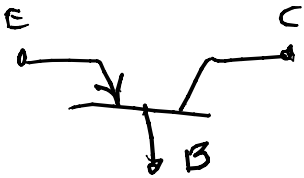
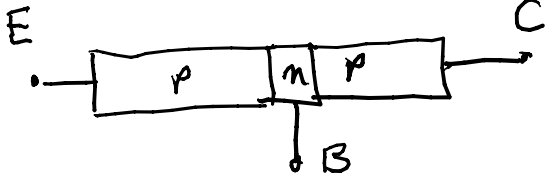
piecewise linear



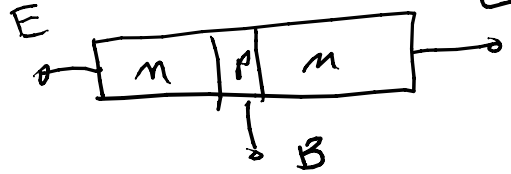
more exact

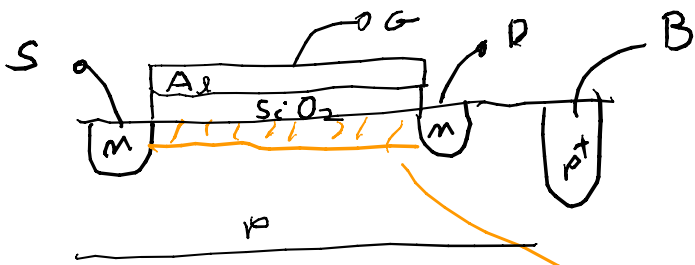


BJT, PNP



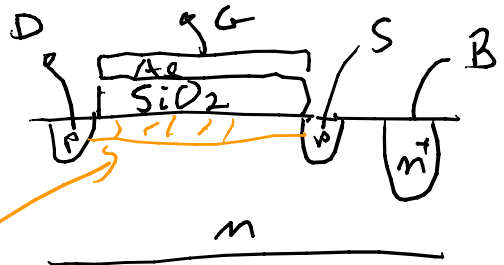
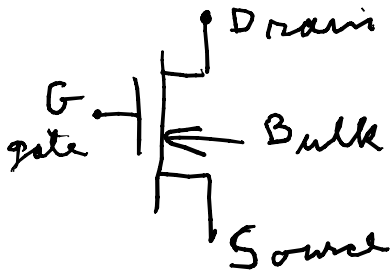
BJT, NPN





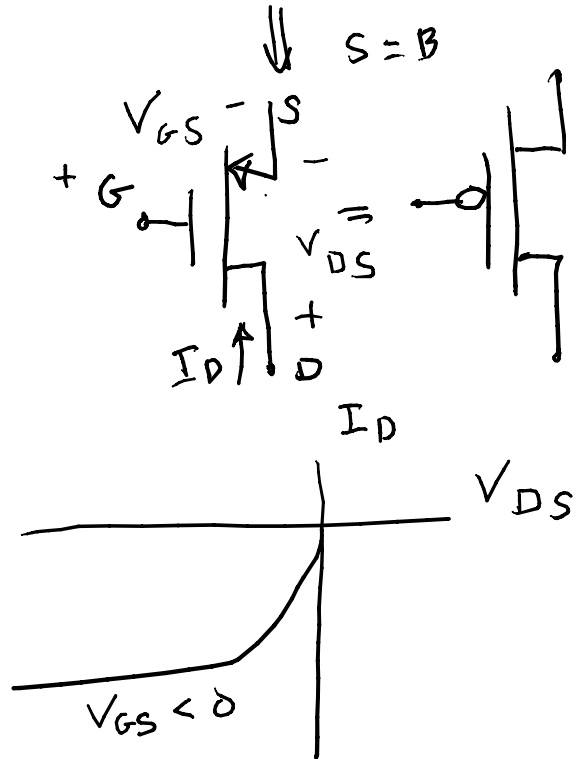
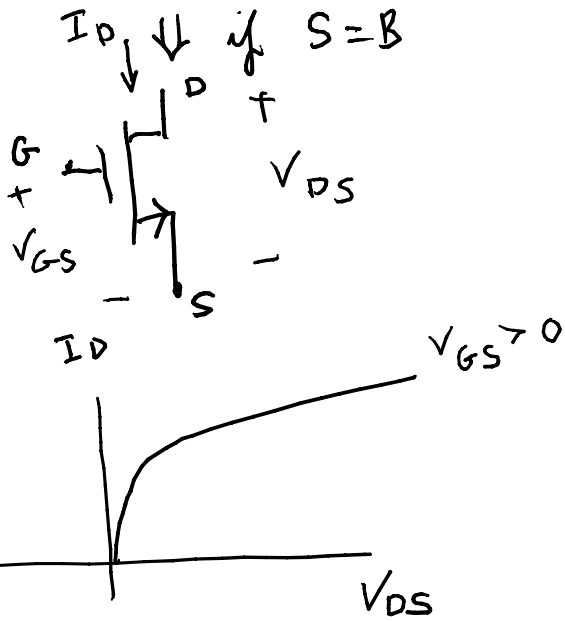
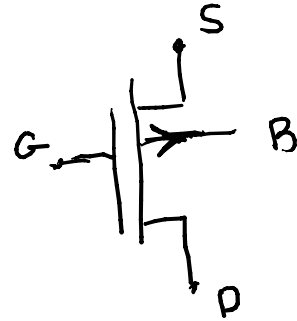
NMOS

||
channel



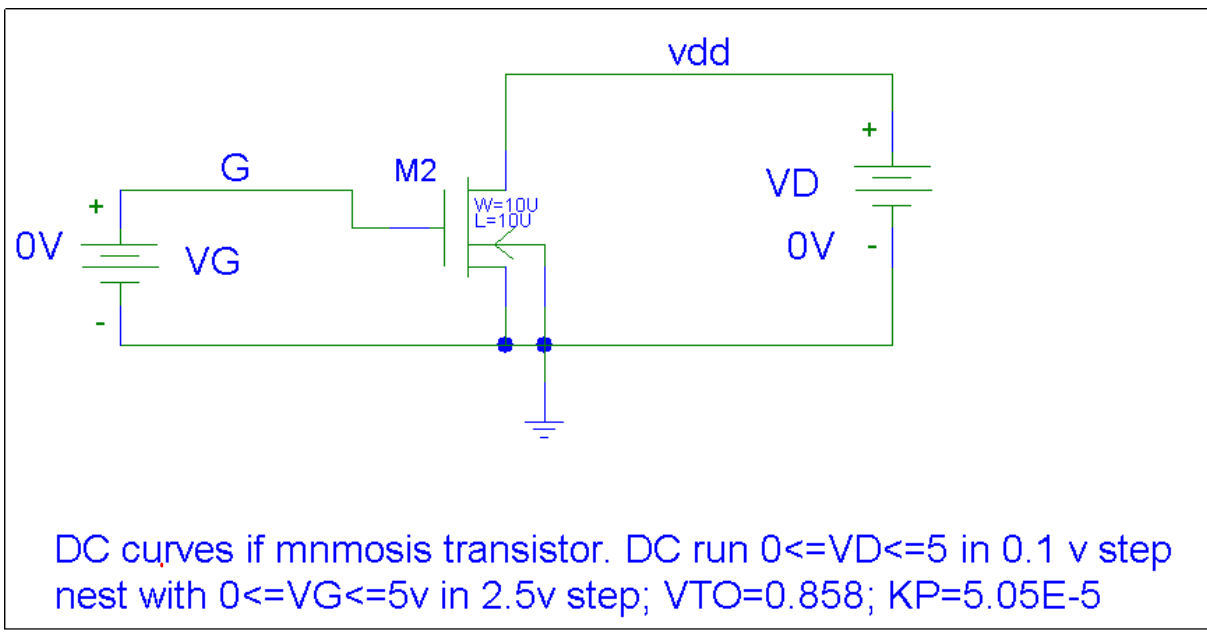
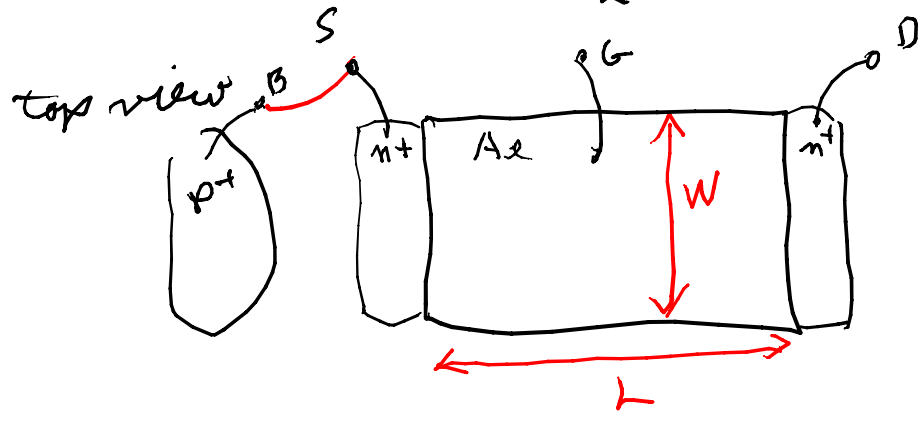
PMOS

channels



Saturation

$$I_D = \frac{K_P}{2} \times \frac{W}{L} (V_{GS} - V_{TO})^2 ; V_{GS} > V_{TO}$$



DC curves if mnmosis transistor. DC run 0<=VD<=5 in 0.1 v step nest with 0<=VG<=5v in 2.5v step; VTO=0.858; KP=5.05E-5

