ENEE 302 Homework Set 5 Due Tu 03/15/05

For CMOS transistors in these problems use the mnmosis and mpmosis transistors with (unless otherwise specified) L=W=10u, Vdd=5V=-Vss. For npn transistors use the BN2X8 mosis transistor.

#1. 30 points (inverter adjustment)

a) For an inverter made with the above CMOS transistors, use KP, VTO and lambda of their models to calculate Wp given Lp=Wn=Ln=10u such that Vout=Vdd/2 when Vin=Vdd/2. Here choose Vss=0.

b) Do a DC run in Spice with Wp as a parameter to find a more precise value of Wp to guarantee Vout=Vdd/2 when Vin=Vdd/2.

#2. 70 points (gate behaviour)

For the two input CMOS NOR and NAND gates shown in Figures 10.12 and 10.13 of page 967 of the text tie all PMOS bulks to Vdd and NMOS bulks to Vss=0. Keep Lp=Wn=Ln=10u

a) Use the values of Wp found in #1 above, check the levels of Y for all combinations of A and B (with a 0 as Vss=0v and a 1 as Vdd=5v). Enter the Y voltage values in a table like the following:

A voltage	B voltage	Y voltage
0	0	
Vdd	0	
0	Vdd	
Vdd	Vdd	

b) Use formulas (10.27) and (10.28) to adjust the widths and lengths and repeat part a).

c) Repeat a) and b) by looking at the 10%-90% rise time when the outputs are loaded by a 20pFd capacitor and in the table Y voltage is replaced by output rise time.

d) Compare the results and give some conclusions on transistor sizing.