ENEE302 HW5 solution
by Y.Z.
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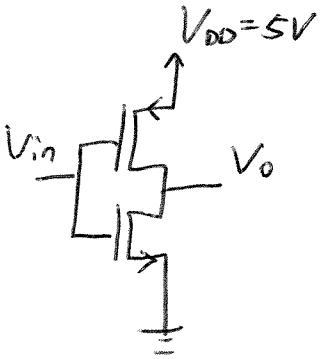
#1. Open BICMOS12.LIB in Wordpad and we find these values.

For NMOS, $V_{to_n} = 0.858\,V$, $KP_n = 5.048E-5$

$\lambda_n = 1.84 \times 10^{-2}$

For PMOS, $|V_{to}|_p = 0.889\,V$, $KP_p = 1.908E-5$

$\lambda_p = 5.01 \times 10^{-2}$




When $V_{in} = \frac{V_{DD}}{2}$, $V_o = \frac{V_{DD}}{2}$

both NMOS and PMOS are in saturation

$I_{Dn} = I_{Dp}$

$$\frac{1}{2}K_{Pn}\frac{W_n}{L_n}(V_{GSN}-V_{ton})^2(1+\lambda_n V_{DSN})$$

$$= \frac{1}{2}K_{PP}\frac{W_P}{L_P}(|V_{GSP}| - |V_{top}|)^2(1+\lambda_P|V_{DSP}|)$$

For NMOS, $V_{GSN} = \frac{V_{DD}}{2}$, $V_{DSN} = \frac{V_{DD}}{2}$

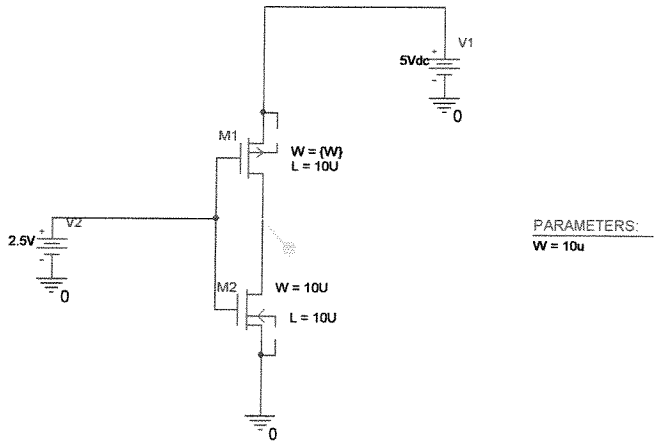
For PMOS, $|V_{GSP}| = \frac{V_{DD}}{2}$, $|V_{DSP}| = \frac{V_{DD}}{2}$

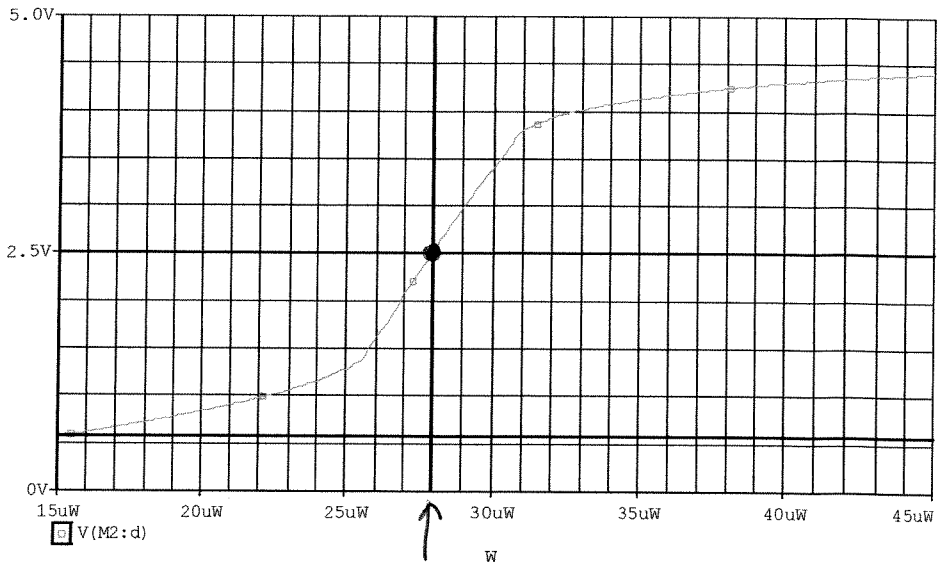
So $$W_P = \frac{K_{PN}}{K_{PP}} \cdot \frac{(\frac{V_{DD}}{2} - V_{tON})^2}{(\frac{V_{DD}}{2} - |V_{top}|)^2} \cdot \frac{(1+\lambda_n \frac{V_{DD}}{2})}{(1+\lambda_P \frac{V_{DD}}{2})} \cdot W_n$$

$= 25.5\,\mu m$

(b)

Do a DC run on the global parameter W from 15μm to 45μm. From measurement on this graph, W=28 μm for Vout=2.5V

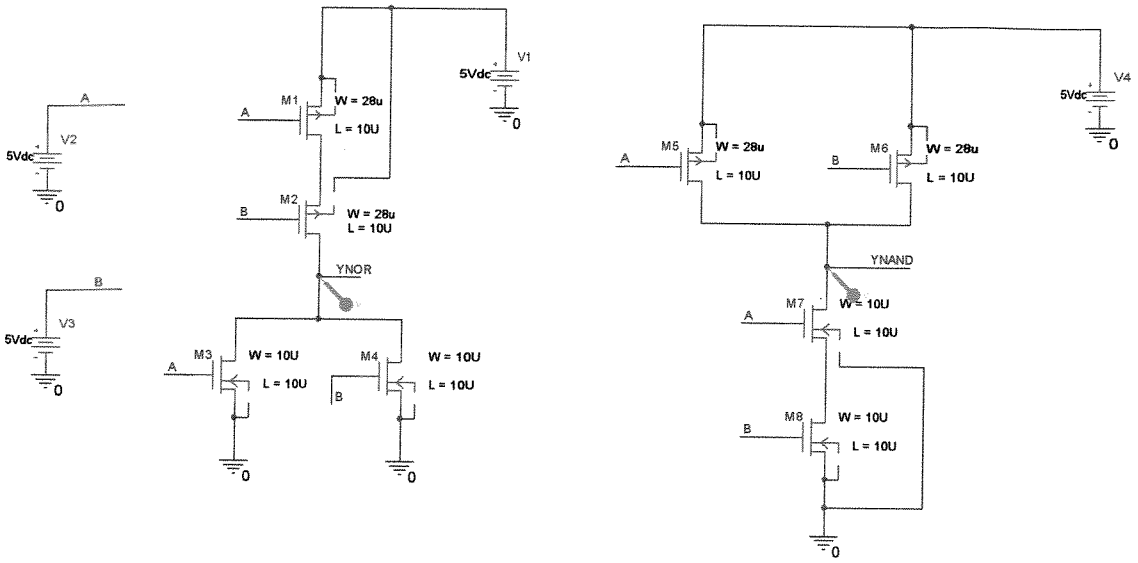



28um

#2.

(a)




For Wp=28μm and Wn=10μm in all transistors, do DC bias run, and read the voltage displaced at the schematic page. Change the voltage A and B values according to the following table, and write down the results for the two gates.

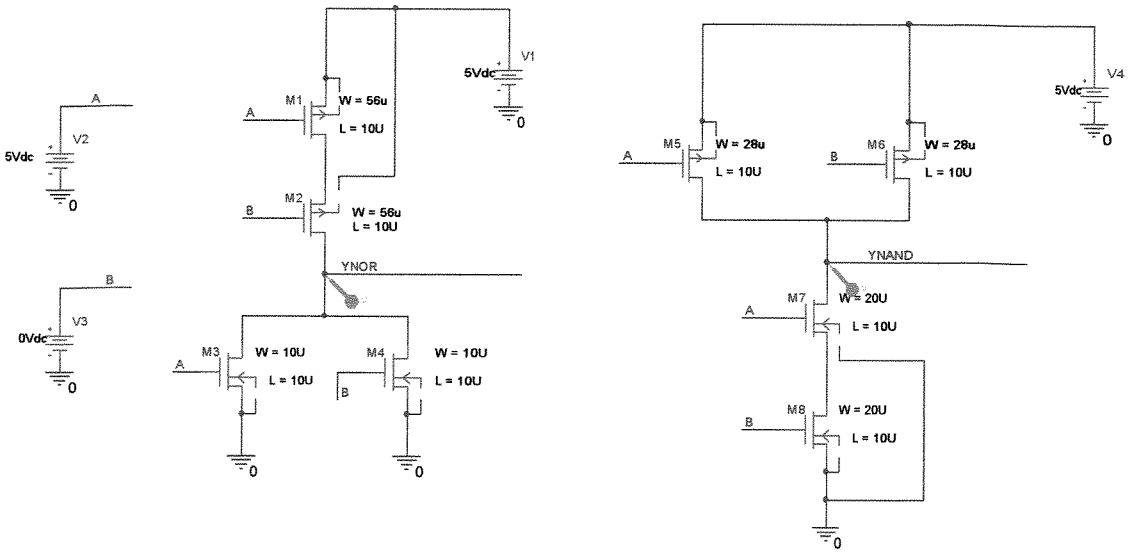
| A voltage | B voltage | Y voltage for NOR gate | Y voltage for NAND gate |
|---|---|---|---|
| 0 | 0 | 5V | 5V |
| 5V | 0 | 84.4nV | 5V |
| 0 | 5V | 38.9nV | 5V |
| 5V | 5V | 17.3nV | 155nV |

(b) According to the formulas, we know that for transistors in parallel, $\left(\frac{W}{L}\right)_{eq} = n \cdot \frac{W}{L}$

for transistors in series, $\left(\frac{W}{L}\right)_{eq} = \frac{1}{n}\frac{W}{L}$

So for the series connection of PMOS in NOR gates and NMOS in NAND gates, we

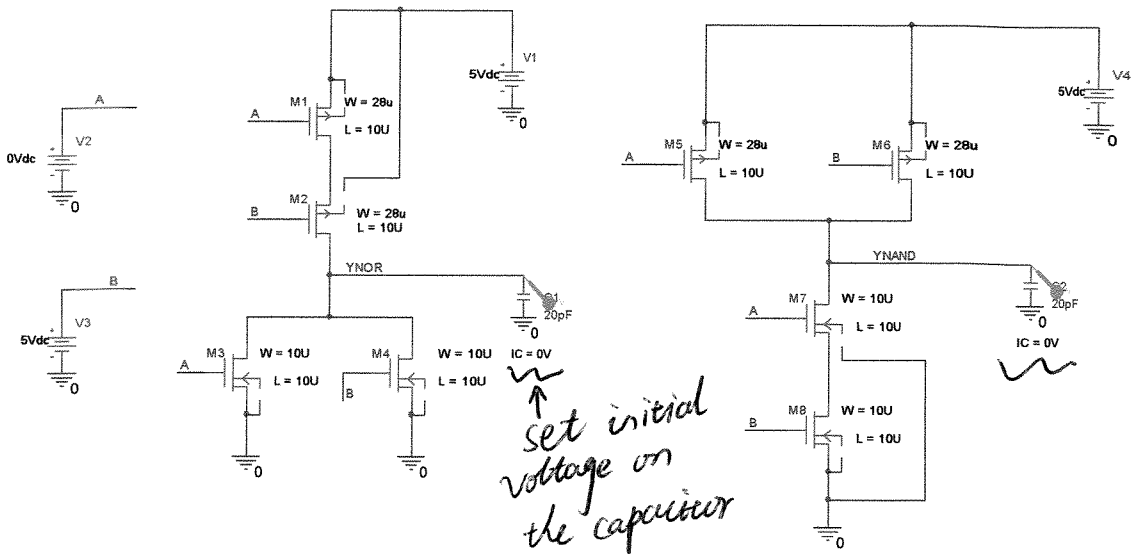
need to double the width of the transistors to achieve an equivalent width the same as in a basic inverter.
For the parallel connections, we keep the width to be the same as in a basic inverter. Because in the worst case, only one of the parallel transistor will be conducting. In order for the current-drawing capability to be no less than the basic inverter, we need to keep the original size.




For Wp=56μm, Wn=10μm in NOR and Wp=28μm, Wn=20μm in NAND, do DC bias run, and read the voltage displaced at the schematic page. Change the voltage A and B values according to the following table, and write down the results for the two gates.

| A voltage | B voltage | Y voltage for NOR gate | Y voltage for NAND gate |
|---|---|---|---|
| 0 | 0 | 5V | 5V |
| 5V | 0 | 40nV | 5V |
| 0 | 5V | 40nV | 5V |
| 5V | 5V | 20nV | 77nV |

(c)

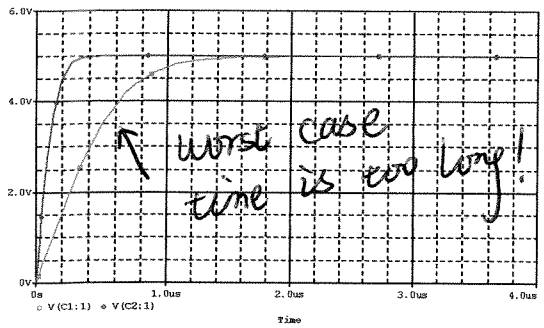



Connect a 20pF capacitor as the load. For Wp=28μm and Wn=10μm in all transistors

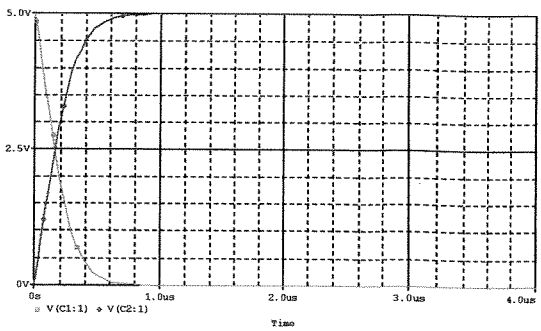
| A voltage | B voltage | Rise time or fall time for Y at NOR | Rise time or fall time for Y at NAND |
|---|---|---|---|
| 0 | 0 | 750ns (rise time) | 180ns (rise time) |
| 5V | 0 | 338ns (fall time) | 361ns (rise time) |
| 0 | 5V | 338ns (fall time) | 361ns (rise time) |
| 5V | 5V | 176ns (fall time) | 690ns (fall time) |

Rise time is the 10% to 90% rise time (the time it takes the output to rise from 10% of the final value to 90% of the final value). Fall time is the 90% to 10% fall time (the time it takes the output to fall from 90% of the final value to 10% of the final value). The graph corresponding to each A, B combination is listed below. The rise time and fall time in the above table are measured from these graphs.

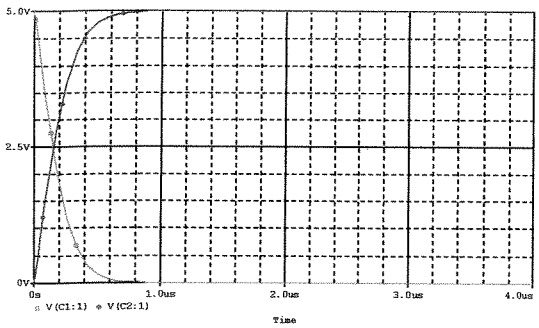
For measuring of a rise time, set the initial voltage on the capacitor to be 0V. (IC=0V)
For measuring of a fall time, set the initial voltage on the capacitor to be 5V. (IC=5V)



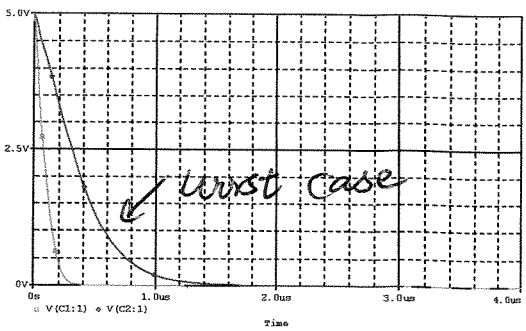

A=0, B=0




A=5V, B=0

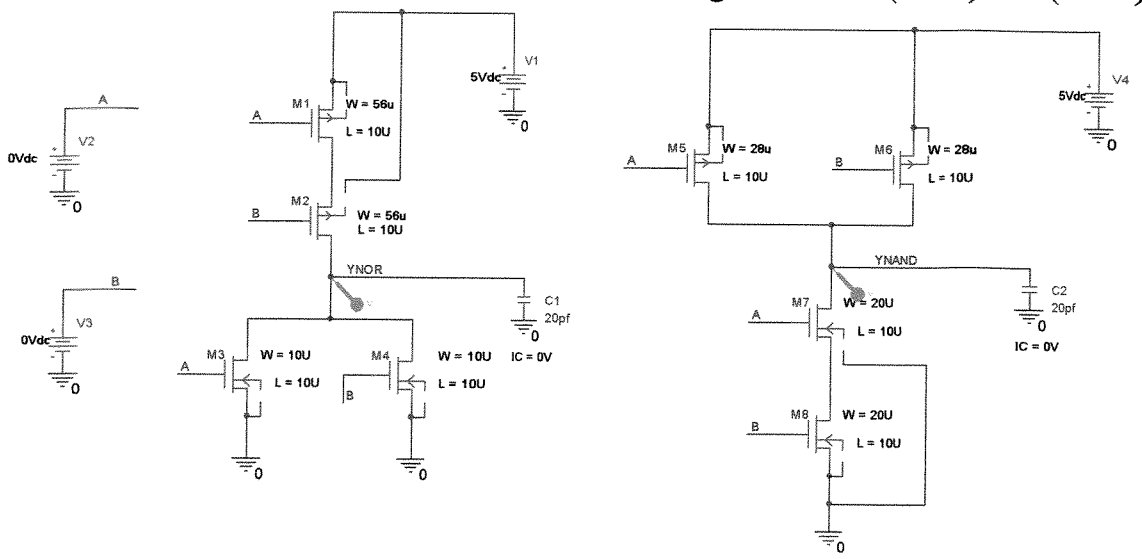



A=0, B=5 V




A=5V, B=5V

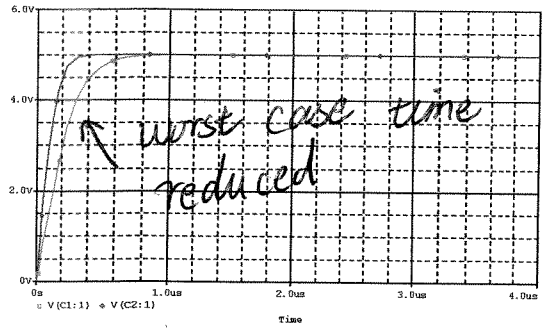
Now change the width of PMOS and NMOS according to formulas (10.27) and (10.28),



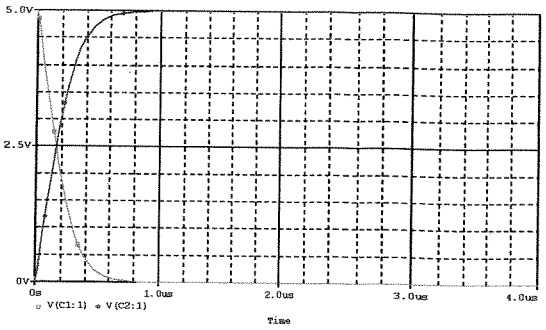

Connect a 20pF capacitor as the load. For Wp=56μm, Wn=10μm in NOR and Wp=28μm, Wn=20μm in NAND

| A voltage | B voltage | Rise time or fall time for Y at NOR | Rise time or fall time for Y at NAND |
|---|---|---|---|
| 0 | 0 | 369ns (rise time) | 187ns (rise time) |
| 5V | 0 | 354ns (fall time) | 368ns (rise time) |
| 0 | 5V | 348ns (fall time) | 354ns (rise time) |
| 5V | 5V | 171ns (fall time) | 343ns (fall time) |

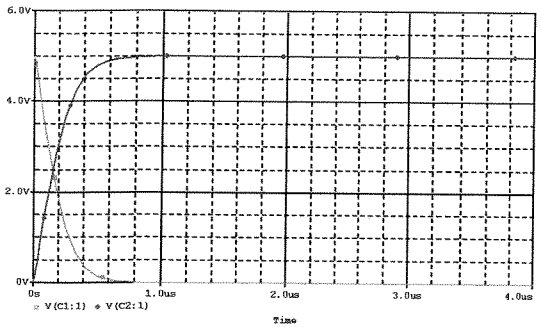
Rise time is the 10% to 90% rise time (the time it takes the output to rise from 10% of the final value to 90% of the final value). Fall time is the 90% to 10% fall time (the time it takes the output to fall from 90% of the final value to 10% of the final value). The graph corresponding to each A, B combination is listed below. The rise time and fall time in the above table are measured from these graphs.



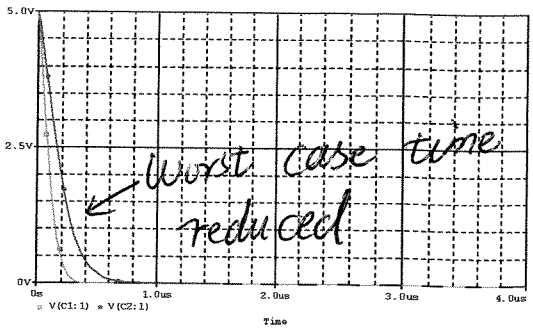

A=0, B=0




A=5V, B=0




A=0, B=5V




A=5V, B=5V

(c) By resizing the transistor in series, the long rising time in the NOR gate when both inputs are low are reduced to that of a basic inverter. The long falling time in the NAND gate when both input are high are also reduced to that of a basic inverter. We see that by transistor sizing, the worst case of rising time or falling time is reduced to that of a basic inverter. This assures that the delay introduced by switching the states for any combination of inputs will be no longer than the switching time of a basic inverter.

Besides this effect on transient behavior, the resizing has little effect on the final voltages of Y for both gates.