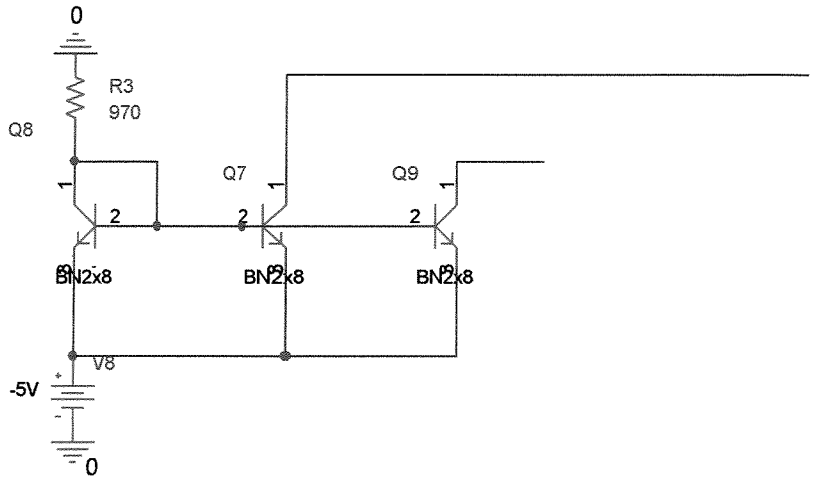
ENEE302 HW4 Solutions Mar 02, 2005

by Y. Z.

#1.

(a)



We want $I_o = 4.3\,mA$.

The total voltage drop across the resistor is 4.3V.

$$I_{ref} = I_C + 2I_B = (1 + \frac{2}{\beta})I_C = (1 + \frac{2}{\beta})I_o$$

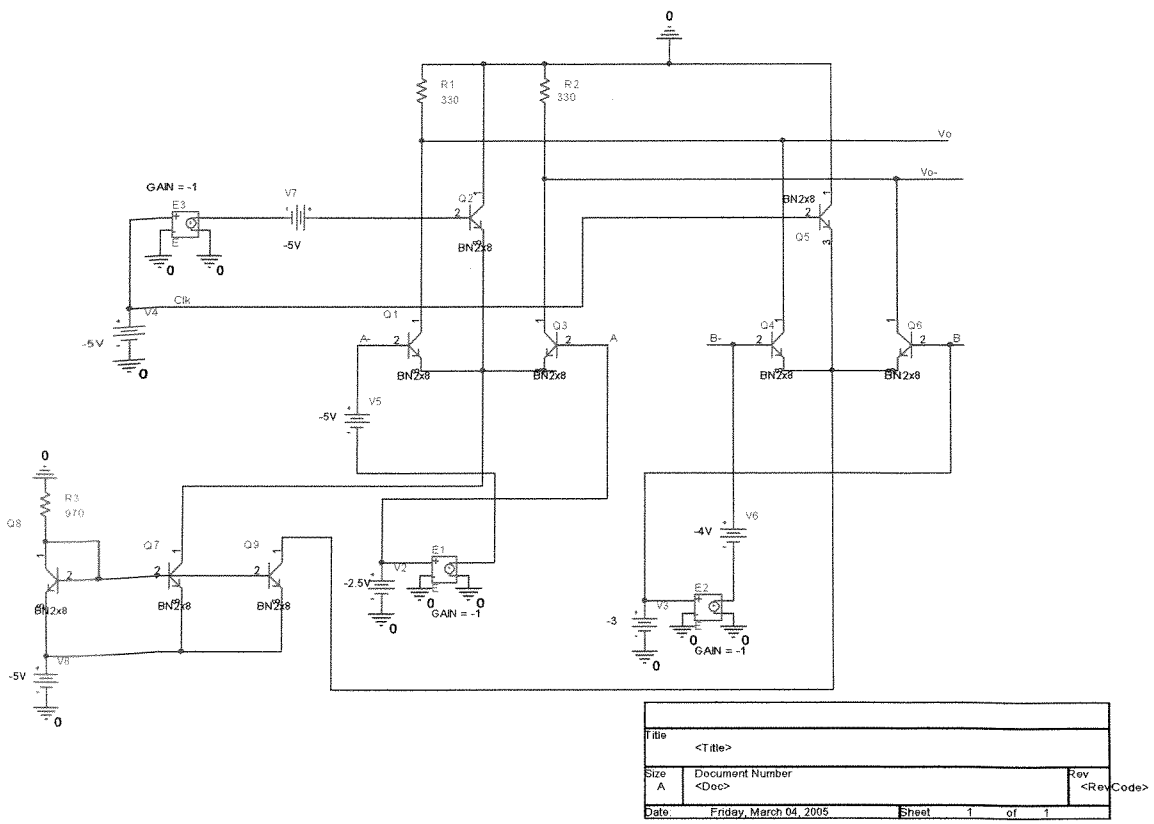
$$= (1 + \frac{2}{100}) \times 4.3mA = 4.38\,mA$$

$$R = \frac{4.3V}{I_{ref}} = \frac{4.3V}{4.38mA} = 980\,\Omega$$

In PSPICE, I find out $R = 970\,\Omega$ gives a better results to 4.3mA. The calculation and simulation agree well.

P2

(b)



I will set VB=-3V for all the simulations. Do a DC sweep on VA, and a parametric run on CLK voltage. If I set CLK=0V, then part A is working and part B bypassed. The inputs of A and A- decide the output voltage. If CLK =-5V, then part B is working and part A is bypassed. The inputs of B and B- decide the output value.

Since the highest voltage in this circuit is zero and the lowest voltage is –5V, my input voltage will vary between –5 and 0V. The A and A- inputs (part A) are biased around –2.5V. For example, if VA=-1V, VA- will be –4V. If VA=-2V, VA- will be –3V. In the schematic, A- are achieved by first inverting A with E component (gain=-1), then adding a voltage drop of 5 V in series. Please see the circuit schematic above for wiring details. The same thing applies to B and B- inputs (part B). We need to do similar things to CLK too. To view more clearly, I will display one curve each time for a different CLK voltage.

In these plots, I will only plot the VA input range from –3.5V to –1.5V, since the circuit works well in this range. This is illustrated in the graph below. I set CLK = 0V and do a DC sweep on VA from –5 to 0V. Here is the Vo and Vo-.

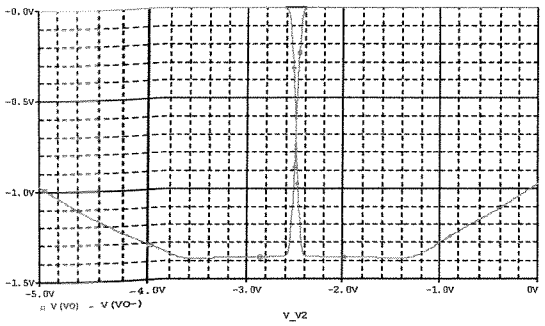


Fig. 1. working ranges

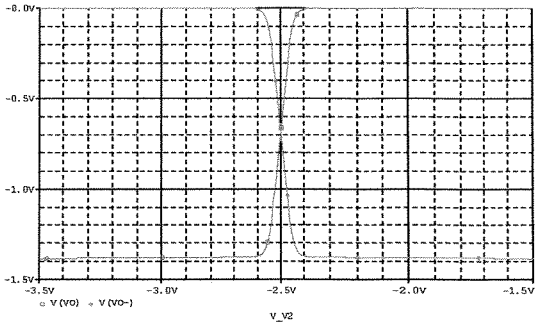


Fig. 2. CLK=0V.

In Fig. 1 we see that in order for the circuit to follow ECL working principle, the input range should be from –3.5 to –1.5 V. Note again for all the following graphs in section (b), I set VB=-3V. In Fig. 2, no current flow in Q2. Part A is operating as ECL circuit. Part B is by-passed since all the current flows in Q5 and no current for Q4 and Q6. In case of Fig 3, since now Q2 is partially conductive, the current that flows through Q3 is not as large as IT when it is turned on. So when A is increased beyond –2.5 V and Q3 is conducting, the voltage drop on RL is smaller than RL*IT. So Vo- is not as low as –RL*IT. Vo is less than 0 V when VA>-2.5 V because now Q4 is conducting current. Fig. 4 can be explained by the same reason as in Fig.3. In Fig. 5, both Q2 and Q5 are conducting, and it is complex to analyze the circuit. This situation is not important for circuit operation since the CLK normally jumps between the highest voltage and the lowest voltage. These intermediate CLK values are seldom used. In Fig. 6, since CLK is low, part A is by-passed. The output is totally decided by part B. Since VB is at low level (less than –2.5V), the VO is high (0 V) and VO- is low (-1.3 V). Fig. 7 is in the same situation as in Fig. 6. Only part B counts.

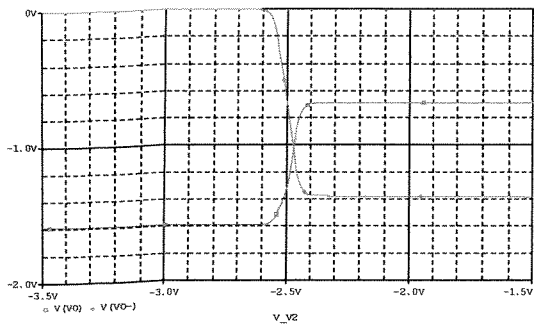


Fig. 3. CLK=-1V

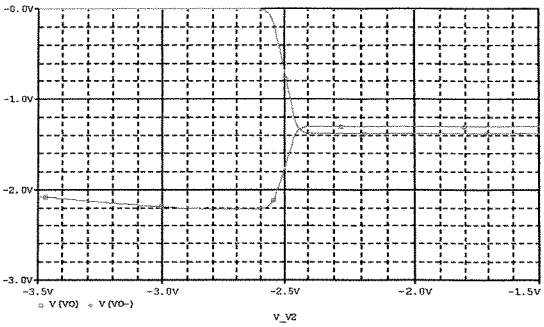


Fig. 4. CLK=-2V

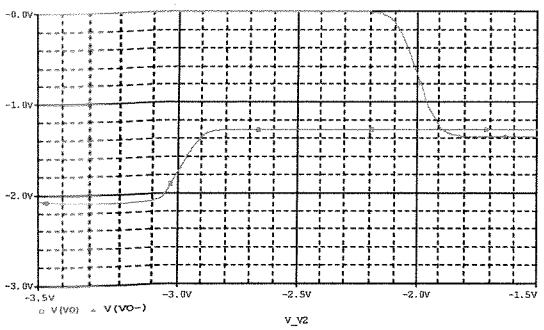


Fig. 5. CLK=-3V

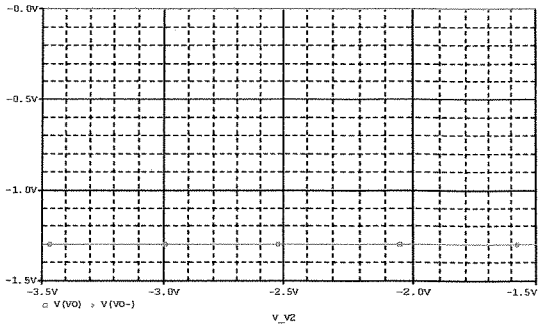


Fig. 6. CLK=-4V

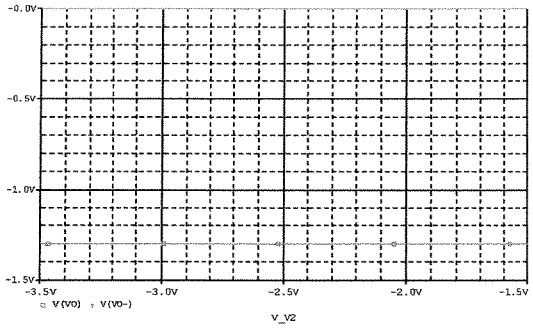
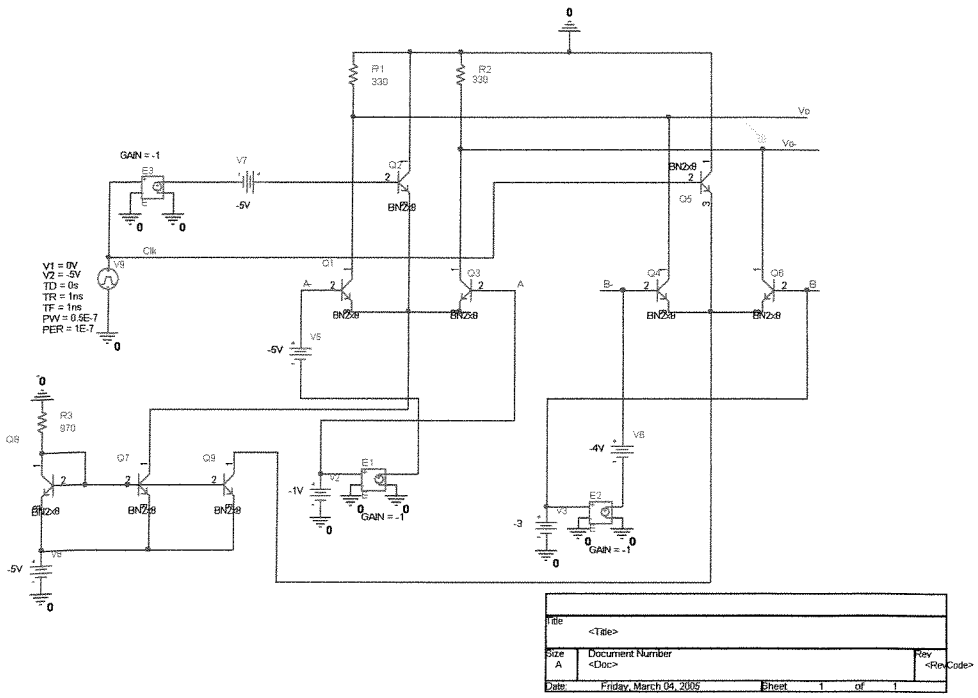


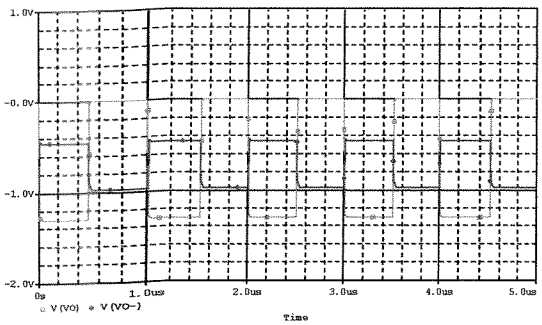
Fig. 7. CLK=-5V

(c)

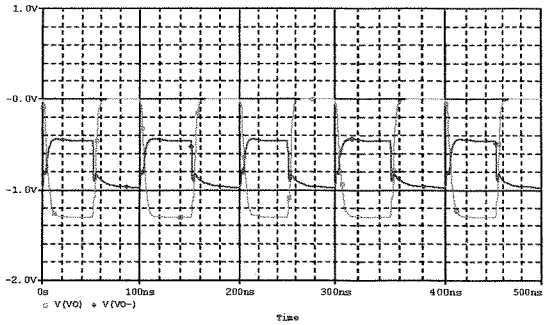


In part C, I use VPULSE for CLK signals, and VB=-3V for all simulations. I do a transient analysis with voltage at A as a parameter. To view more clearly, I will show them in separate graphs. I will start with VA=0V. In all graphs below, VPULSE starts from the –5V half cycle.

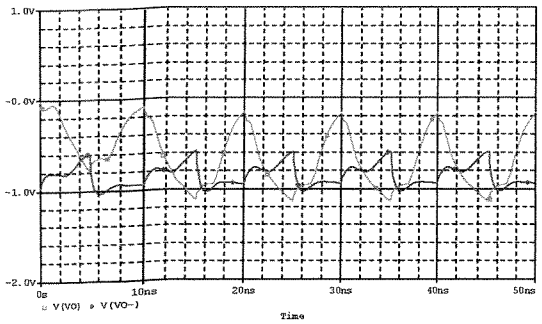
VA=0V, VB=-3V



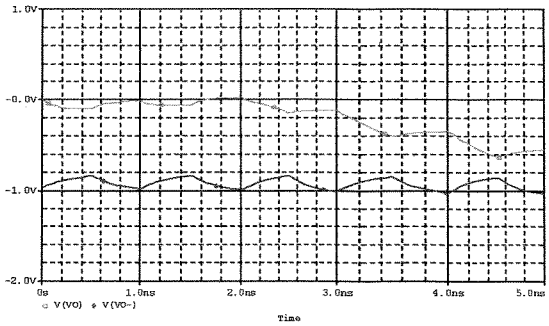
CLK 1MHZ



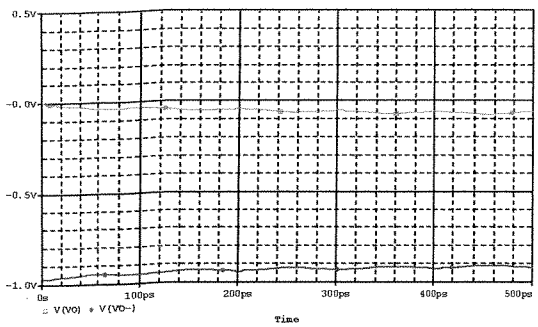
CLK 10MHz



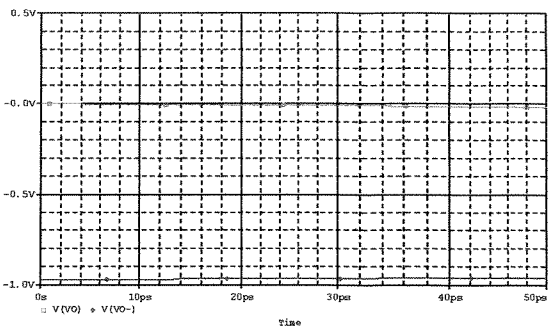
CLK 100MHZ



CLK 1GHz

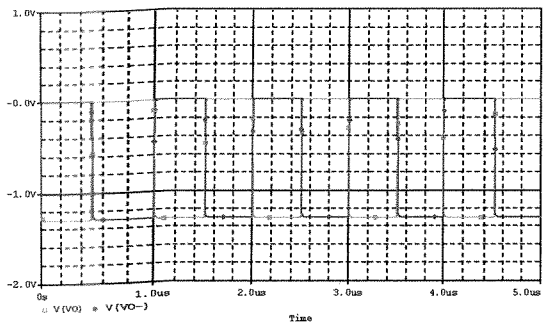


CLK 10GHz

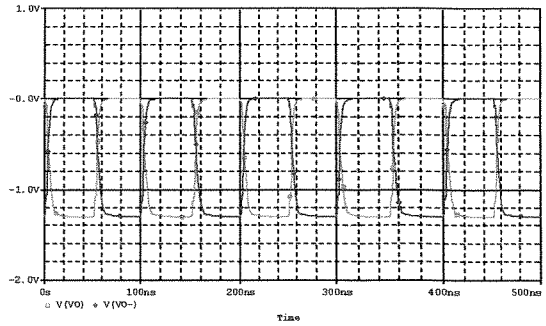


CLK 100GHz

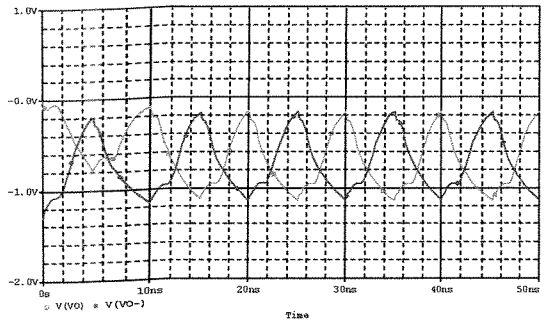
VA=-1V, VB=-3V



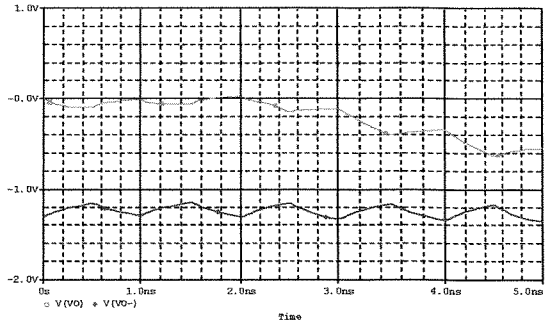
CLK 1MHZ



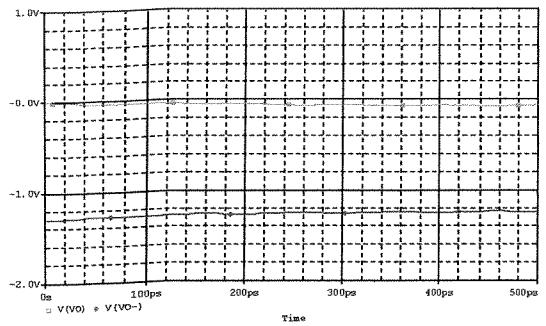
CLK 10MHz



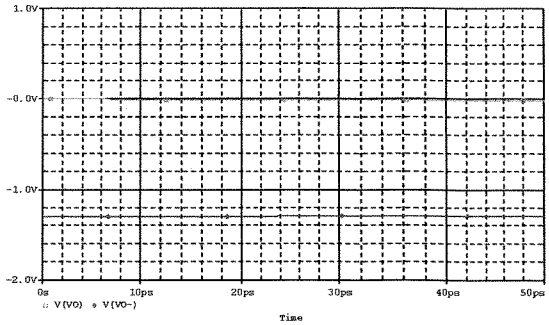
CLK 100MHZ



CLK 1GHz

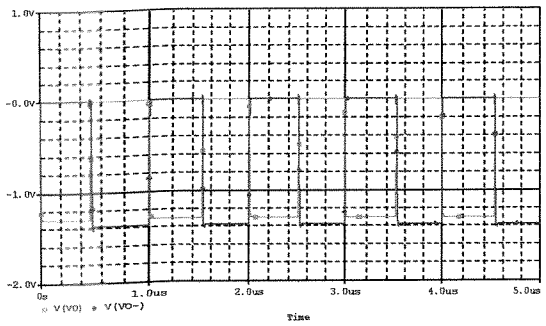


CLK 10GHz

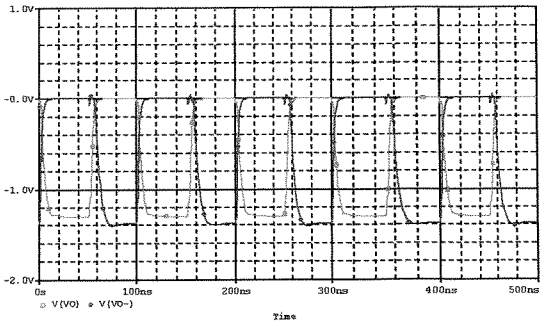


CLK 100GHz

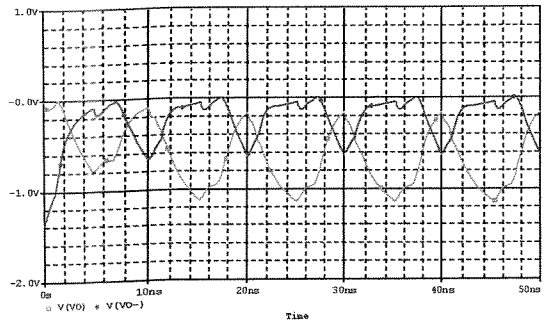
VA=-2V, VB=-3V



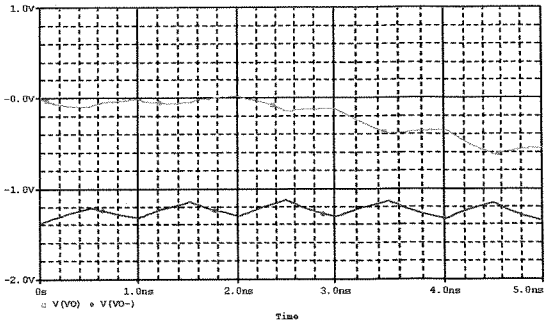
CLK 1MHZ



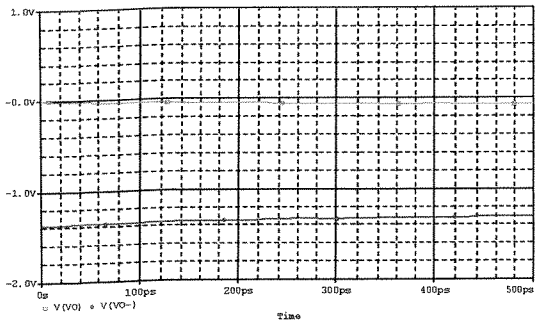
CLK 10MHz



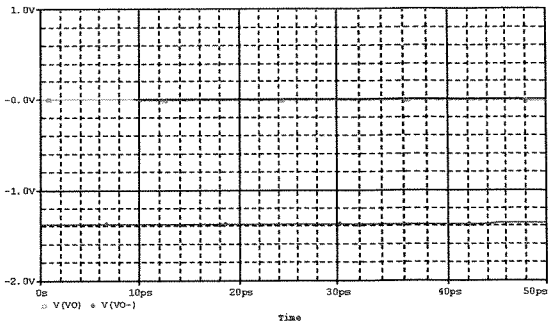
CLK 100MHZ



CLK 1GHz

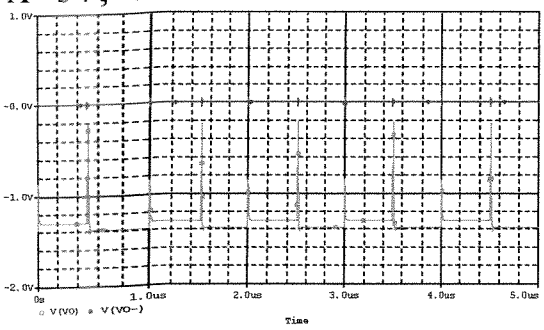


CLK 10GHz

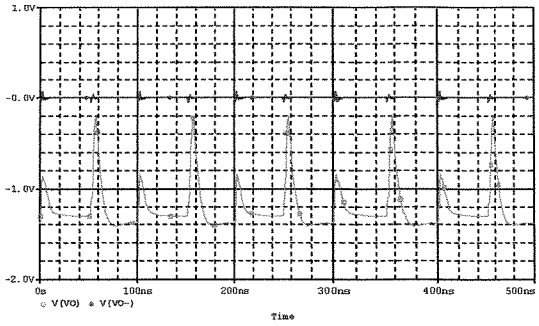


CLK 100GHz

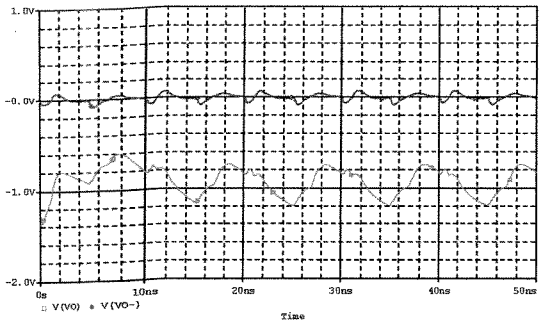
VA=-3V, VB=-3V



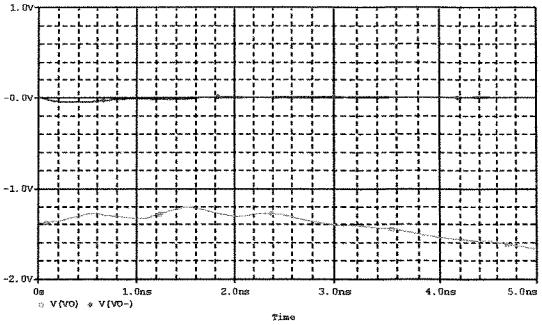
CLK 1MHZ



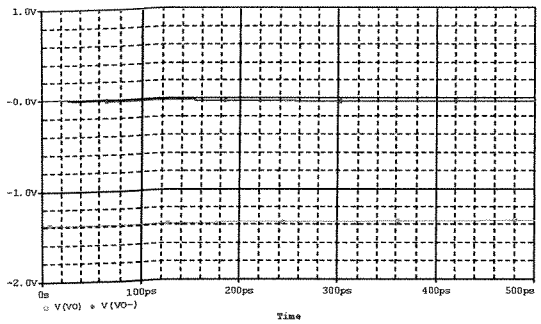
CLK 10MHz



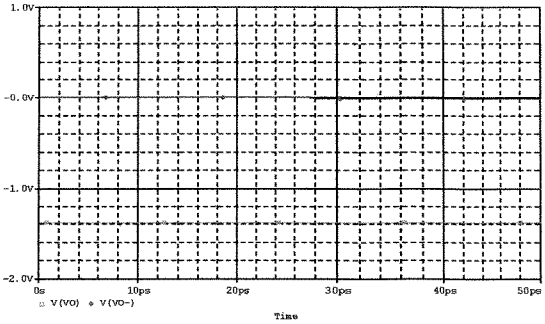
CLK 100MHZ



CLK 1GHz

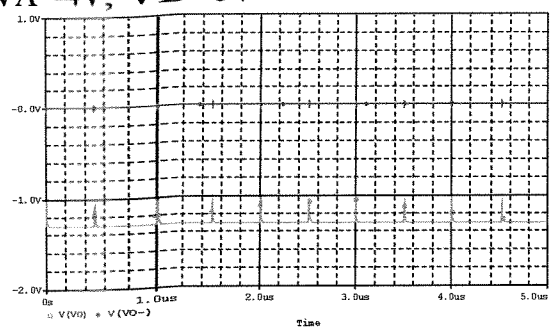


CLK 10GHz

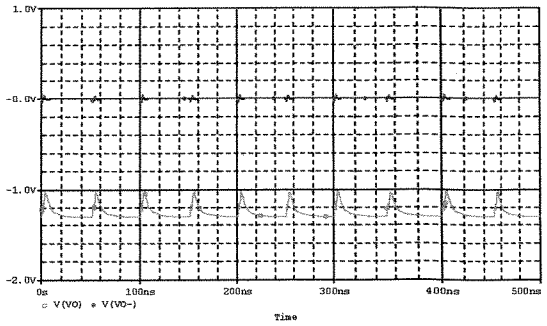


CLK 100GHz

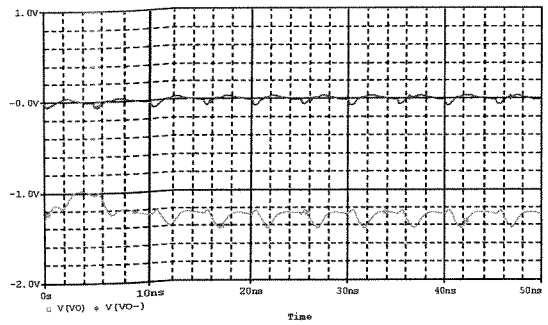
VA=-4V, VB=-3V



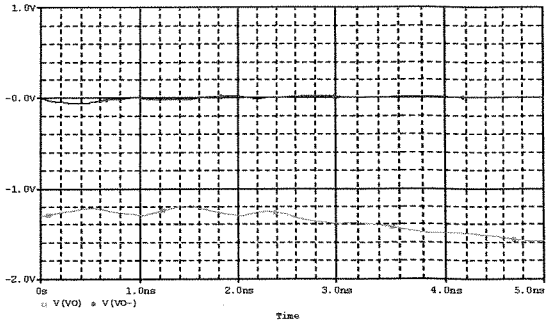
CLK 1MHZ



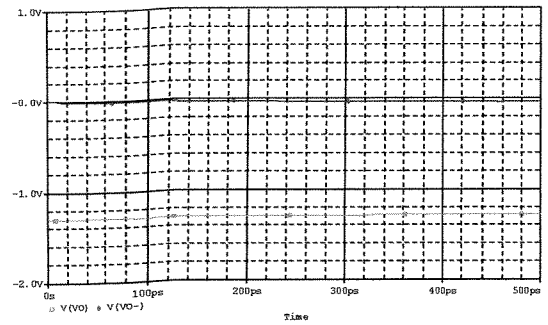
CLK 10MHz



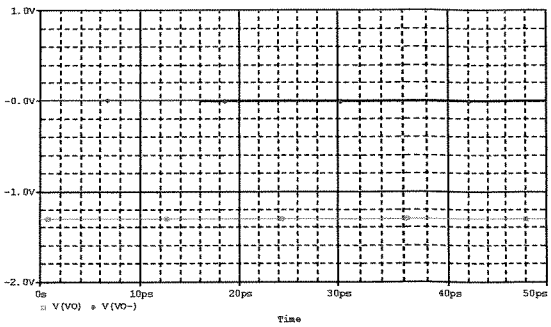
CLK 100MHZ



CLK 1GHz

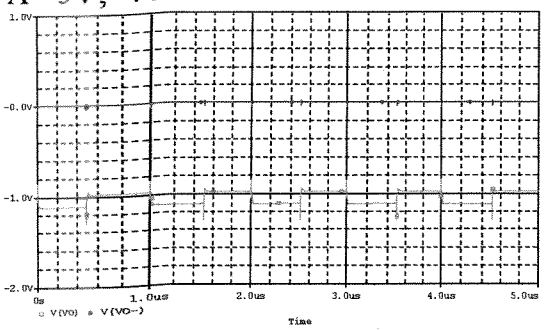


CLK 10GHz

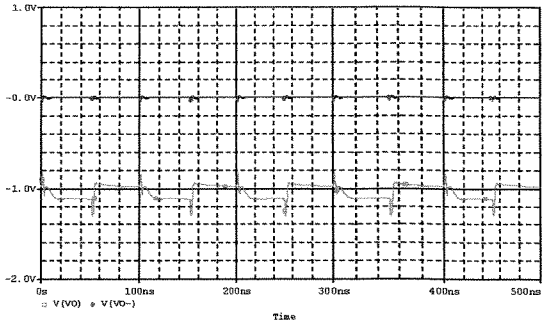


CLK 100GHz

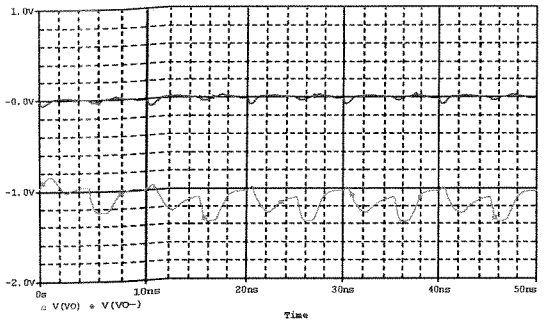
VA=-5V, VB=-3V



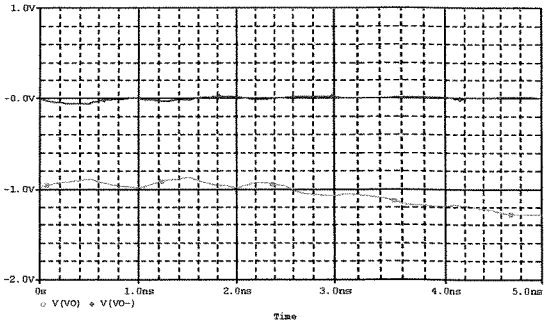
CLK 1MHZ



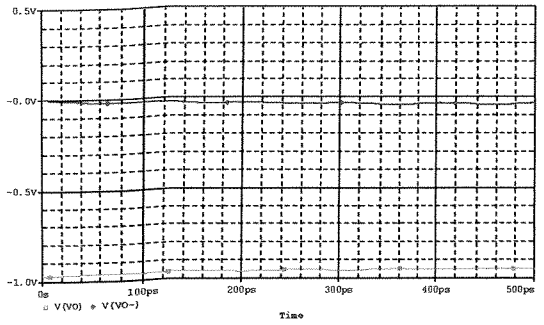
CLK 10MHz



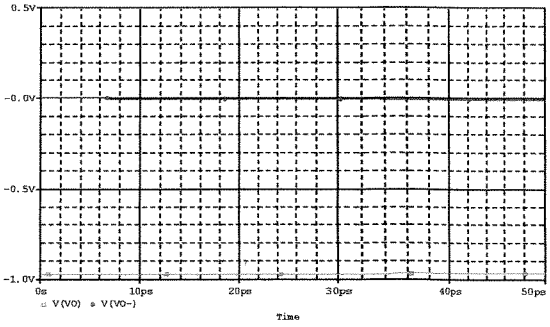
CLK 100MHZ



CLK 1GHz



CLK 10GHz



CLK 100GHz

(d)

A multiplexer is a circuit in which information from many sources is switched in a defined order to be sent to a single destination. In this circuit, the switching is controlled by the complementary CLK signals. When CLK is 0V, Q5 is turned on and all current from the right current source flows through Q5. No current will flow through Q4 and Q6 no matter what the inputs are to these two BJTs. If CLK is 0V, CLK- will be –5V. Q2 is shut down and cannot affect the operation of Q1 and Q3 as a ECL differential pair. So when the CLK is high (0V), the two output voltages Vo and Vo- are solely determined by the inputs to part A. Based on the same mechanism, when CLK is low, the two output voltages are solely determined by the inputs to part B.

When CLK is high, we now analyze how part A is working. Since the whole circuit has a maximum supply voltage of 0V and a minimum supply voltage of –5V, the differential inputs to the differential pairs should be biased around –2.5V, which means the common mode input voltage is –2.5V. If node A is connected to (–2.5+Δx) V, node A- should be connected to (–2.5-Δx) V. Since part A and part B are exactly symmetrical, the same thing will apply to part B. When the voltage of node A is higher than –2.5 V, Q3 is conducting current and the voltage at Vo- will drop to –I*R. Q1 is not conducting and the voltage at Vo is kept at 0V. So the high output voltage of the circuit is 0 V, and the low output voltage is –I*R.

If the voltage at node A keeps increasing, Q3 will enter the saturation region (Vbase>Vcollector). The collector current of Q3 will decrease, and the output voltage Vo- will increase from –I*R as shown in part (b) Fig 1. If the voltage at node A is too much below –2.5 V, the voltage at node A- will be too high above –2.5V. Transistor Q1 will enter the saturation region and the output Vo will deviates from -I*R. So the input range cannot go from –5V to 0V. From Fig. 1 in part (b), we observe that the input range is from –3.6V to –1.4V. Only in this range, the circuit fully follows the ECL working principle. From the examples in part (b), we see that in order to get a perfect multiplexer, the CLK signal should switch between 0V and –5V, so Q2 or Q5 can be fully shut down or fully turned on.

The frequency response of the circuit is studied in part c. When the switching frequency is below 10MHz, the circuit works well as a multiplexer. When the frequency is around

100MHz, the output cannot change as fast as the CLK signal switches. When the CLK signal is beyond 1GHz, the circuit cannot function at all. So we conclude that for the circuit to act as a multiplexer, the operating frequency should be below 10MHz.