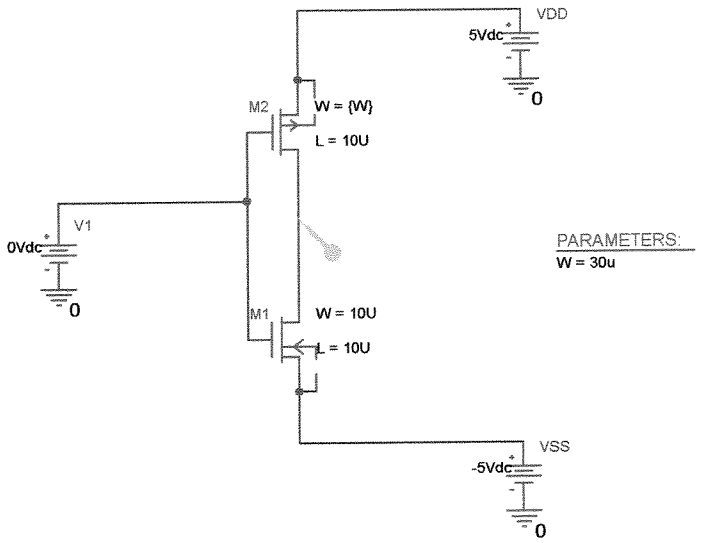
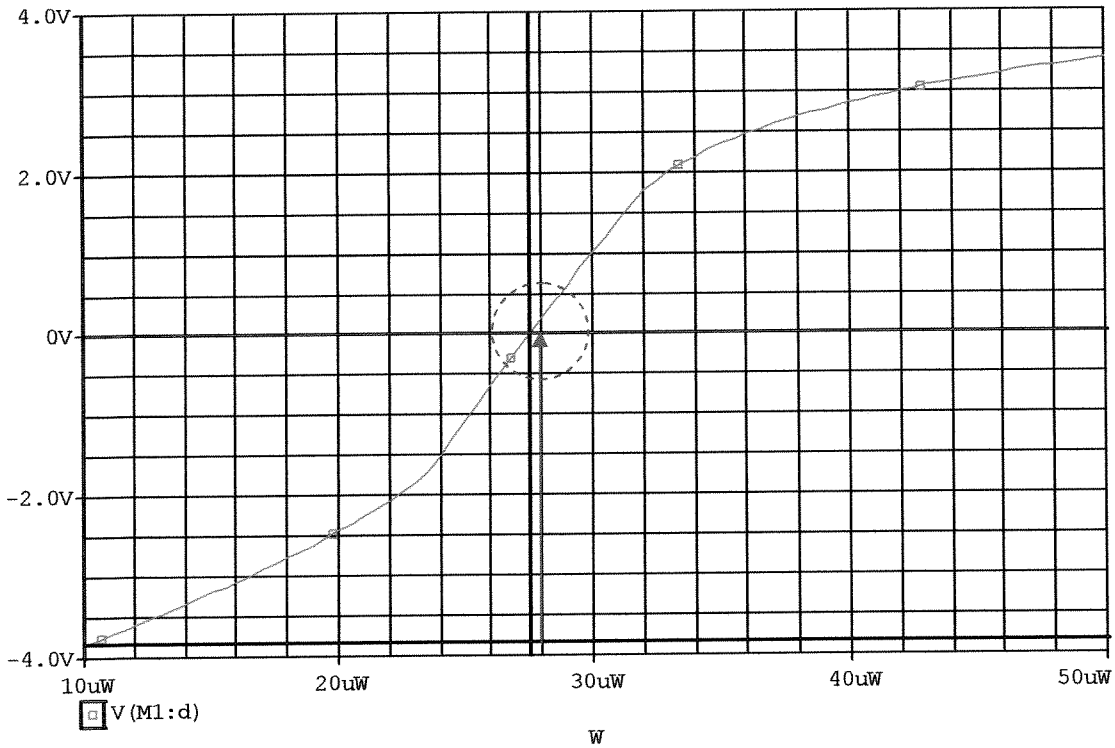
#2.

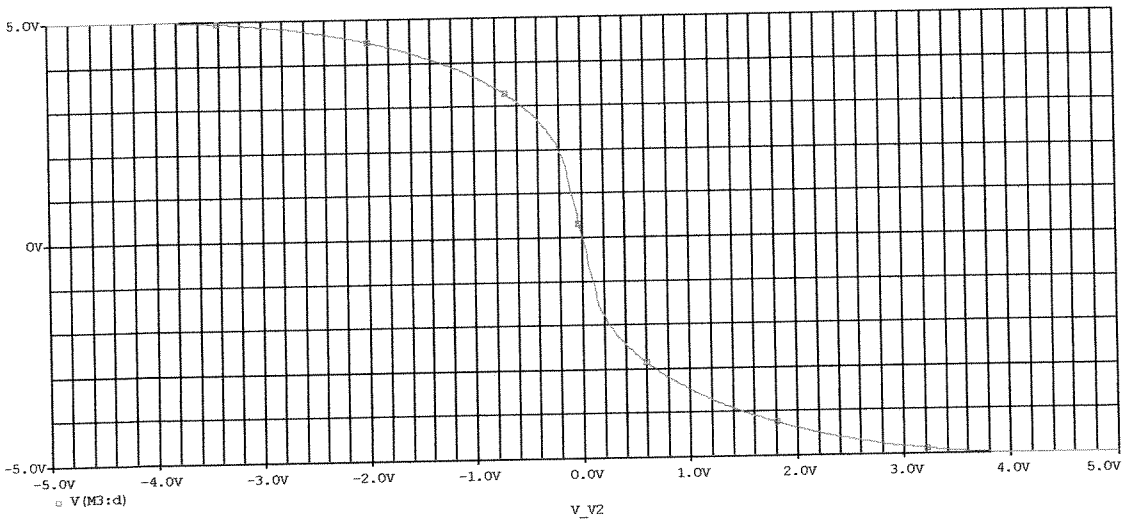
(a) Set V1=0V and the width of the PMOS is a parameter named W. Do a DC sweep with W instead of sweeping any voltage source. Observe the output voltage. The plotted Vo will intersect with the x-axis, which gives us the point where the output voltage is zero. We read the W that makes the Vo=0.
Here is the W. W=27.5 um.





P6

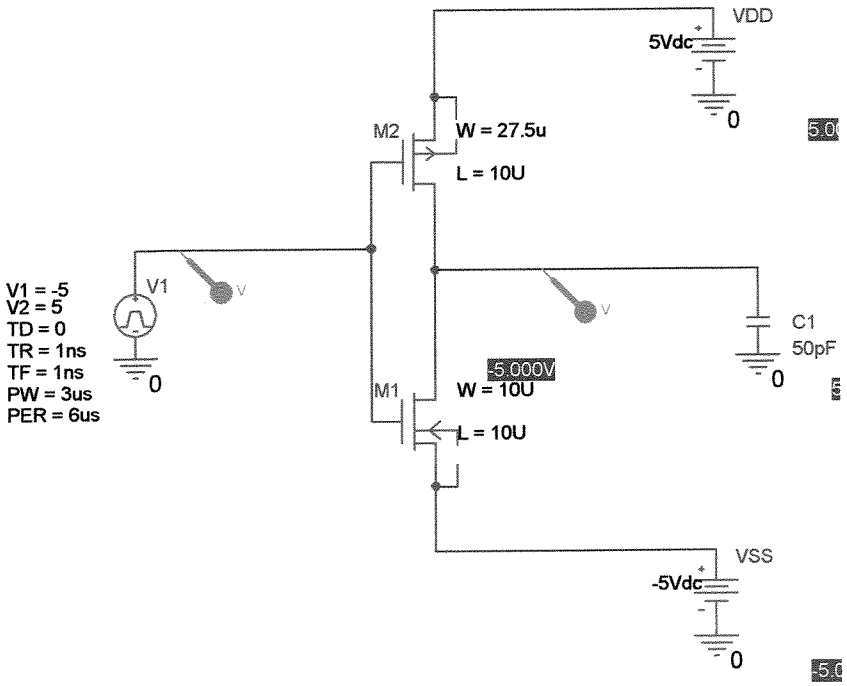
with Wp=27.5um, I plot Vout vs. Vin as below

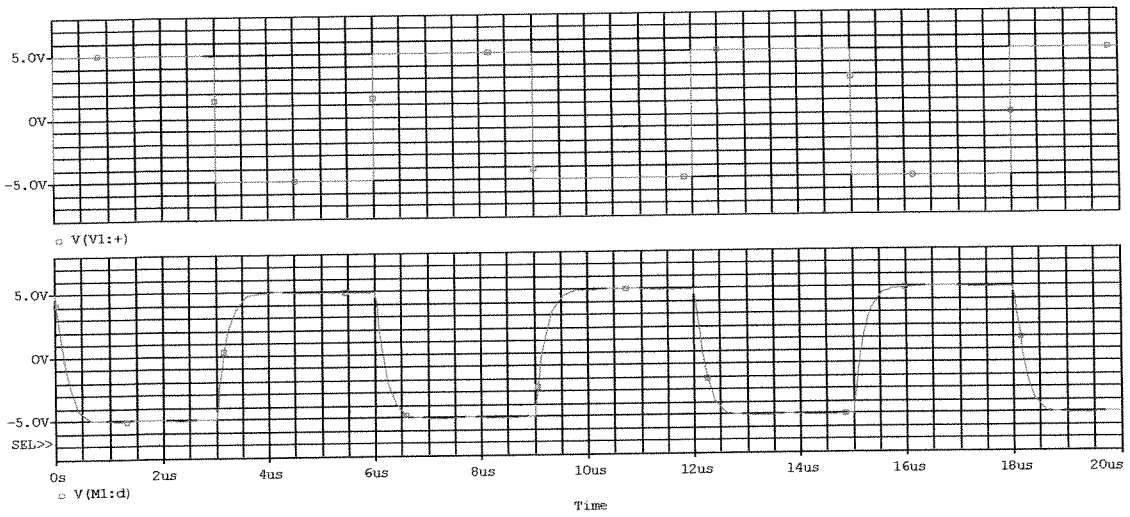


(b):

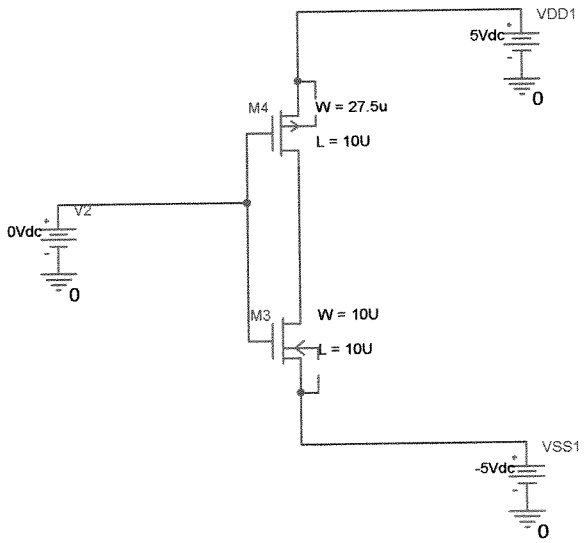
Now insert C=50pF. To get Fig 4.57, we need to do a transient analysis over time to observe the output voltage with a capacitor load. For a transient analysis, we need a time-varying voltage source as the input voltage to the inverter. One choice is to use a part named VPULSE in the source library. The properties that we have to define for the VPULSE are as follows:
V1: the first voltage level
V2: the second voltage level
TD: delay time before the first pulse
TR: rise time at the rise edge of the pulse
TF: fall time at the fall edge of the pulse
PW: pulse peak width
PER: the repeat cycle

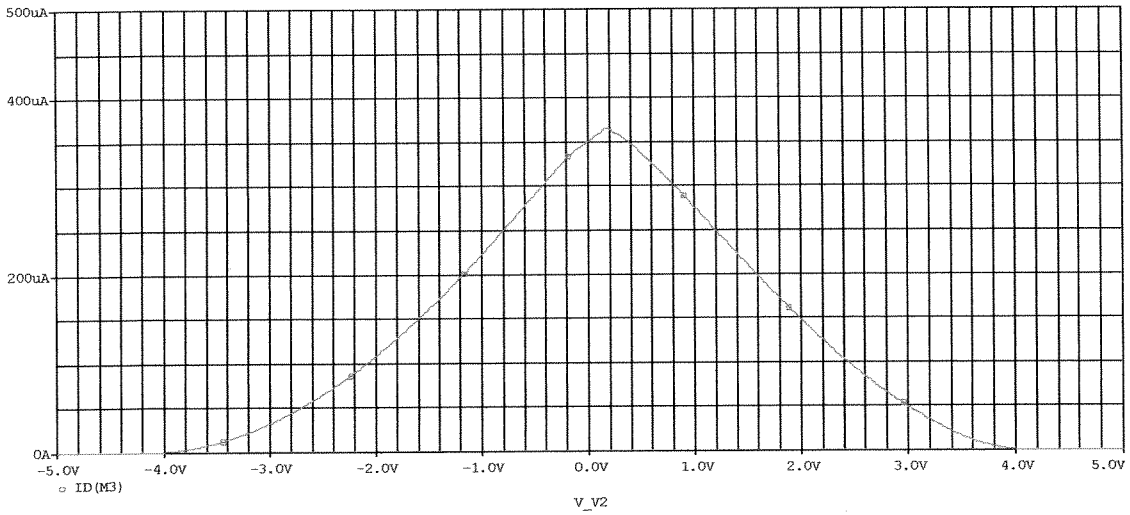
The values I defined are shown in the circuit schematic below. TD and TF are small because I want a nearly perfect square pulse as the input. Note if you set the pulse width too large, you may lose the transient details at the rising and falling edges of the output.





(3) To plot Fig. 4. 58, just detach the capacitor since we are doing a DC sweep. Put a DC voltage source at the gates. Sweep this voltage source from VSS to VDD, and plot the drain current of the NMOS.





With $\lambda = 0$

#3. $V_t = 1V$, $L = 1V$, $\mu_n C_{ox} = 120\ uA/V^2$

$V_{GS1} = 1.5V$.

$$120uA = \frac{1}{2} \times 120 \times \frac{W_1}{1} (1.5 - 1)^2$$

$$\Rightarrow W_1 = 8um$$

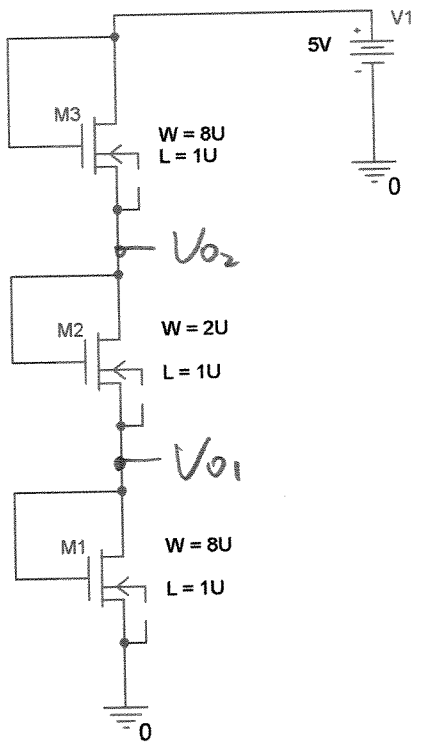
$V_{GS2} = 2V$.

$$120uA = \frac{1}{2} \times 120 \times \frac{W_2}{1} (2 - 1)^2 \Rightarrow W_2 = 2um$$

$V_{GS3} = 1.5V = V_{GS1}$

$\Rightarrow W_3 = 8um$

The circuit schematic to simulate is as below:

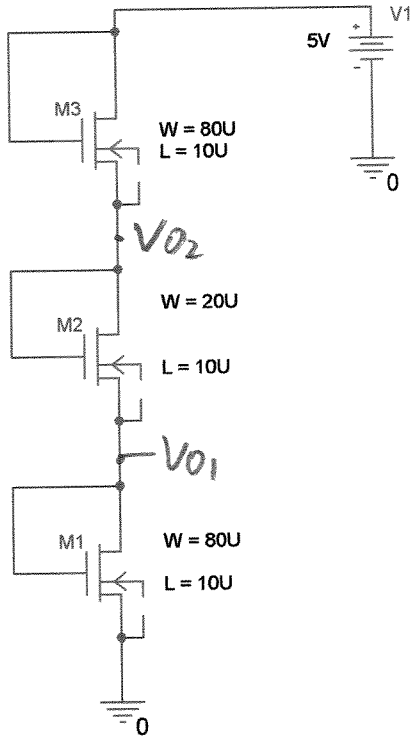


IF we choose the L=1um as in the book, and W1=8um, W2=2um, and W3=8um. We got Vo1=1.325V, and Vo2=3.675 V.

Now we simulate the circuit again but with L=10um (shown in the graph below). To keep W/L the same, we use W1=80um, W2=20um, and W3=80um. We got Vo1=1.325V, and Vo2=3.546 V.

The result has discrepency because in the simulated transistor, we have different K_n and V_{TO}. They are not as given by the problem in the textbook.

P11



If $\lambda \neq 0$, I checked in the library BICMOS12.Lib to find λ for nmos (MNMOS1S) is 1.84×10^{-2}.

So now for M1, $V_{GS1} = 1.5\,V$, $V_{DS1} = 1.5V$

$$120\,uA = \frac{1}{2} \times 120 \times \frac{W_1}{1} (1.5-1)^2 \times (1 + 1.84 \times 10^{-2} \times 1.5)$$

$$\Rightarrow W_1 = 7.78\,um$$

For M2, $V_{GS2} = 2\,V$, $V_{DS2} = 2V$

$$120uA = \frac{1}{2} \times 120 \times \frac{W_2}{1} (2-1)^2 \times (1 + 1.84 \times 10^{-2} \times 2)$$

$$\Rightarrow W_2 = 1.92\,um$$

For M3, $V_{GS3} = 1.5\,V$, $V_{DS3} = 1.5\,V$

$$120uA = \frac{1}{2} \times 120 \times \frac{W_3}{1} (1.5-1)^2 \times (1 + 1.84 \times 10^{-2} \times 1.5)$$

$$\Rightarrow W_3 = 7.78\,um$$

For $L = 10\,um$, W should be multiplied by 10.