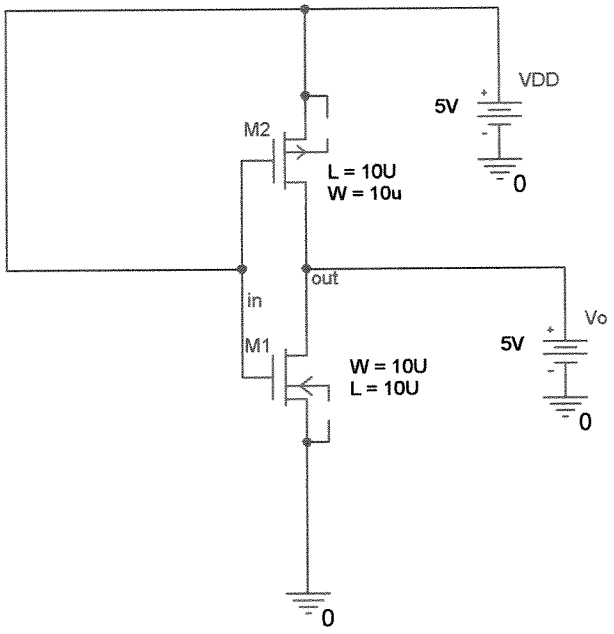
ENEE302 HW 2 Solutions
Feb. 18th, 2005, by Y. Z.

P1

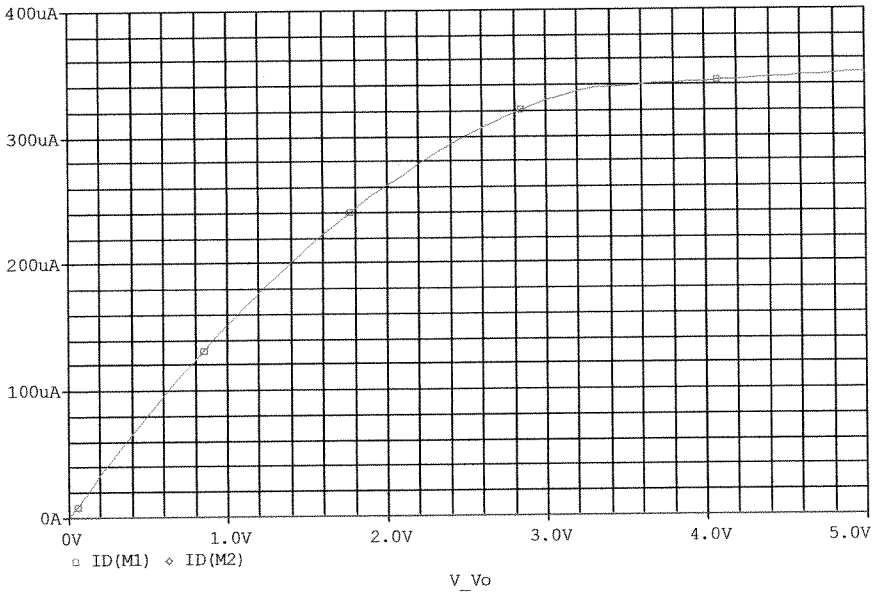
#1.

To plot Figure 4.54 on pp.338, we set up the circuit as below. The input to both gates of the transistors are tied to VDD=5V. Since Vo is the x-axis in the graph, we need to plot the drain current of both transistors against the Vo. So we put a DC voltage source at Vo, and do a DC sweep on this source from 0 to 5V, with 0.1 V increments.

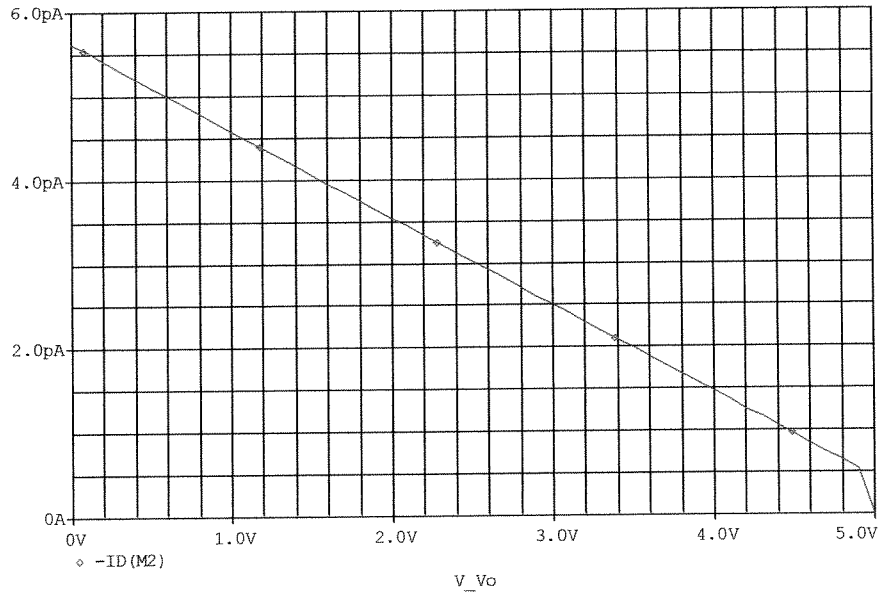


The resulting graph is shown below, same as Fig. 4. 54. The green line is the drain current for NMOS, and the red line (hard to find since it overlaps with the x-axis) is the drain current for PMOS. Since the PMOS is shut down, the drain current of PMOS is very close to zero. To illustrate how small it is, I plot the drain current of the PMOS separately on another graph.

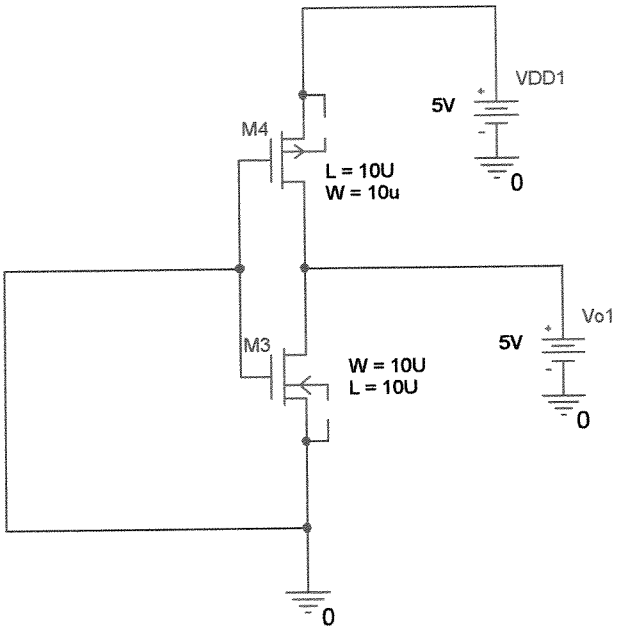
P2



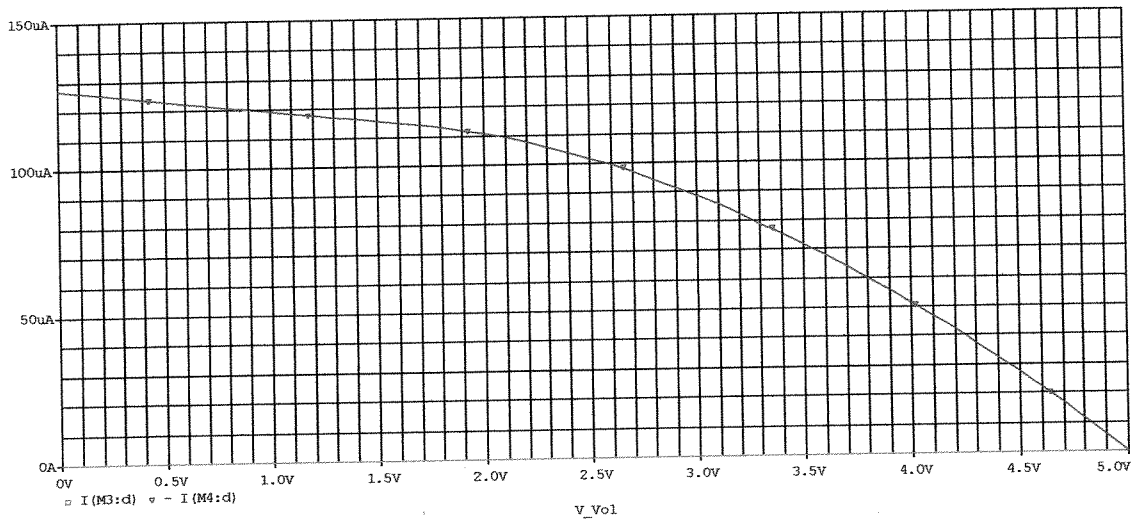
Below is the plot showing the extremely small drain current of the PMOS, which is not shown in the previous plot.

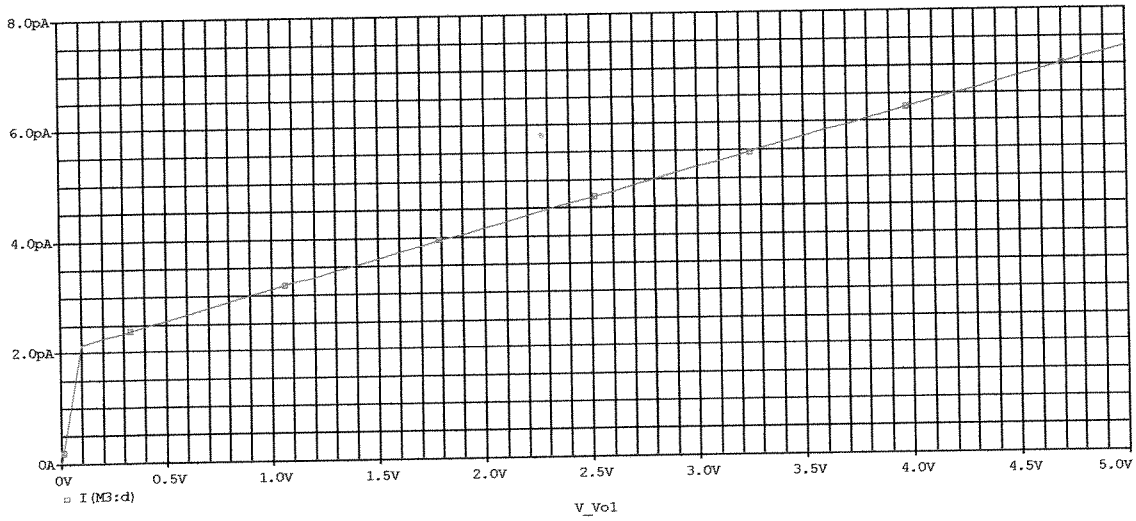


To plot Figure 4.55 on pp.338, we set up the circuit as below. The input to both gates of the transistors are tied to VSS=0V. Since Vo is the x-axis in the graph, we need to plot the drain current of both transistors against the Vo. So we put a DC voltage source at Vo, and do a DC sweep on this source from 0 to 5V, with 0.1 V increments.



The resulting graph is shown below, same as Fig. 4. 55. The green line is the drain current for NMOS (hard to find since it overlaps with the x-axis), and the red line is the drain current for PMOS. Since the NMOS is shut down, the drain current of NMOS is very close to zero. To illustrate how small it is, I plot the drain current of the NMOS separately on another graph.


150uA
100uA
50uA
0A
0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
I(M3:d)
- I(M4:d)
V_Vol


8.0pA
6.0pA
4.0pA
2.0pA
0A
0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
I(M3:d)
V_Vol