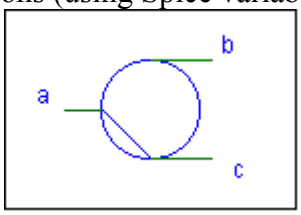
ENEE 302 Final Exam Spring 2005

Work all problems and show your work for partial credit. 100 points, 120 minutes; if stuck be sure to go on to the next problem. Your signature guarantees the work is your own - only signed exams will be graded. Open book, open notes; Unless otherwise stated, for MOS transistors assume that $3KPn=5KPp=300uA/V^2$, $VTOn=0.75VTOp=1.3V$, $\lambda n=\lambda p=0$. Good luck

1. [30 points, 30 minutes]

A new nanotechnology field effect transistor, nanoFET, has the following schematic symbol with the model equations (using Spice variable conventions) given below.

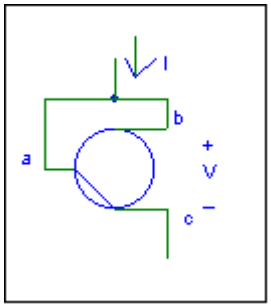


$$i_a = C_a \frac{dv_{ac}}{dt}$$

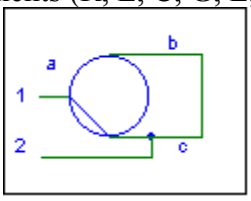
$$I_b = -I_c = \beta \frac{(V_{ac})V_{bc}}{1+\lambda|V_{bc}|}$$

a) For $\lambda=0.001/mV$, $\beta=1nA/mV^2$, and $Ca=0.1pFd$, sketch the DC curves of I_b/β versus V_{bc} over $-5mV<V_{bc}<+5mV$ with V_{ac} as a nested voltage in 2mV volt steps from $-2mV<V_{ac}<2mV$

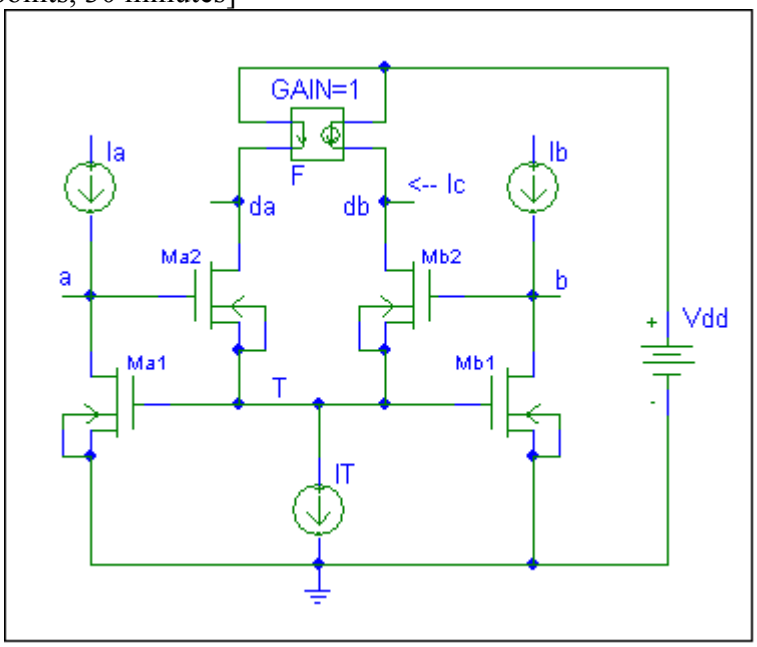
b) The nanoFET of part a) is connected as shown next. Sketch the DC I versus V curve for this connection giving asymptotes and behavior near V=0.



c) The nanoFET of part a) is connected as shown next. Give the PSpice equivalent circuit for the component seen between nodes 1 and 2 in terms of the PSpice components (R, L, C, G, E, F).



2. [35 points, 30 minutes]



For the above circuit assume that all transistors are equal with W=L and when turned on are in saturation. Assume that a digital one is represented by I=1ma and a digital zero by I=0mA. Assume also the tail current IT=1mA and sufficiently large λ_n.

a) When Ia=Ib, for both 1mA and 0mA, give the output current Ic..

b) Using |Ic| to represent the digital output, give a truth table using Ia and Ib as inputs.

c) Determine if this is a suitable current mode logic gate. If so, what gate is it? And if not give the reason why not.

3. [35 points, 30 minutes]

For the following circuit, both transistors are identical with W=L; Vi and Vo are measured with respect to ground

a) Determine for what Vi the two transistors are turned on and in saturation.

b) Determine analytically, at DC, Vo versus Vi for the Vi found in part a) and sketch the resulting curve for those Vi falling within the range Vss=-5V<Vi<+5V=Vdd.

c) Is this a good digital logic inverter (of CMOS type inverter)? A good small signal analog inverter (of op-amp type inverting amplifier)? Explain.