ENEE 302 Homework Set 3 Due Tu 03/16/04 (revised from 03/09/04)

for all these problems use the mnmosis and mpmosis transistors

#1. 25 points (inverter design and loading)

a) Using Vdd=-Vss=5V and Wn=Ln=Lp=10u design a CMOS inverter such that Vin=0 gives Vout=0. Record Wp.
b) Load this inverter with a capacitor C_L (from the output to ground) of default value 10pFd and for parametric runs, 10pFd to 210pFd in 50pFd steps. Check Vout for Vin=0 for all C_L.
c) To the loaded inverter of b) apply a positive pulse of period 10uS and 50% duty cycle and amplitude Vdd with rise time 1nS (starting at 0V and fall time (falling to 0V). Plot in PSpice the resulting transient response output and input with C_L as a parameter.
d) Keeping C_L in place feed Vout into another inverter with an identical load C_L and repeat the runs of c).

#2. 25 points (XOR in CMOS)

a) Using the CMOS transistors found in #1, design a two input XOR circuit as per Fig. 10.15, p. 969, but with the ground replaced by Vss. Connect all substrates to the CMOS sources. Check in PSpice by appropriate pulses that the XOR is realized.

b) Connect all PMOS substrates to Vdd and all NMOS substrates to Vss and recheck to see if the XOR is still realized.

#3. 25 points (XOR in PTL)

Repeat both parts of problem #2 above for the pass-transistor logic of Fig. 10.31 when the circuit is loaded by a 10pFd capacitor.

#4. 25 points (domino gate)

Implement the single input domino logic circuit of Fig. 10.37, p. 997, replacing the transistor ground by Vss and using the CMOS transistors found in problem #1 above (tie all PMOS substrates to Vdd and all NMOS ones to Vss). Keep the capacitors grounded; use 10pFd ones, and make a PSpice probe plot as per Fig. 10.37(b).