Work all problems and show your work for partial credit. 100 points, 120 minutes. Your signature guarantees the work is your own - only signed exams will be graded. Open book, open notes; Assume that 5KPp=3KPn=250uA/V², -VTOp=1.5VTOn=0.3V, - γ p=5 γ n=0.05V^{1/2}, ϕ f=0.3V, Vdd=5V 1. [45 minutes, 50 points]



For the above circuit

a) Find Wn and Wp for Mn and Mp such that V(ref)=Vdd/2. For this minimize the current in Mn consistent with Wn no smaller than 5 microns.

b) Assuming V(ref)=Vdd/2 find Wns and Wps for Mns and Mps such that as current sink and source their drain currents are 0.2ma in magnitude. State any assumptions used. 2. [45 minutes, 50 points]

The following circuit is typical of those in pass transistor gates or track and hold circuits. Here Vc is a clock assumed to have a 60% duty cycle, its high voltage being Vdd and its low being at ground; Cl=20pF and Rl=100K are the load. Assume that at the start, t=0=0+, both the clock and the initial capacitor voltage are 0, Vc(0)=0=v(0) and that the clock transitions from 0 to Vdd at t=T1=10mS.



- a) Sketch one period of the clock voltage Vc(t).
- b) When is node a the source? When is it the drain?
- c) At t=0+ give the state of the transistor (cutoff, saturation, or Ohmic).
- d) What is the maximum value of voltage, vmax, that the output v could ever attain and how could it be achieved?
- e) Set up the differential equations to be solved for the first period of operation; include the body effect represented by γ . Assume that v(t) < vmax over the period.