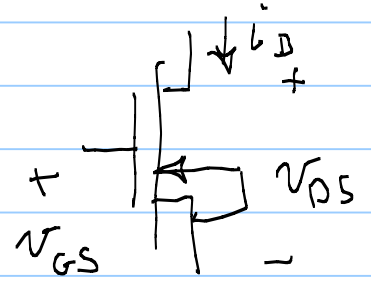
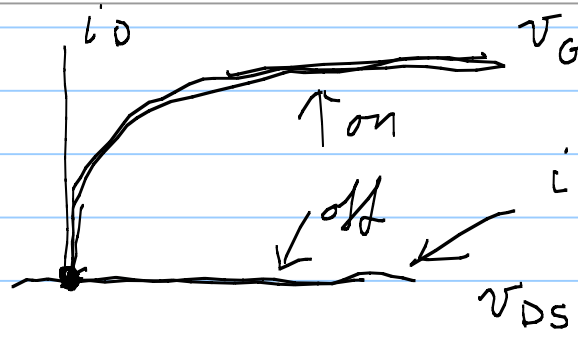
EE302

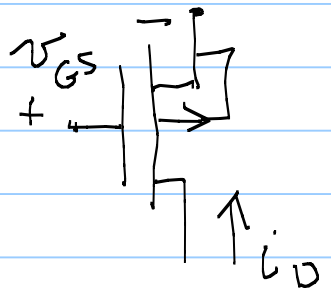
Note Title 2/26/2004



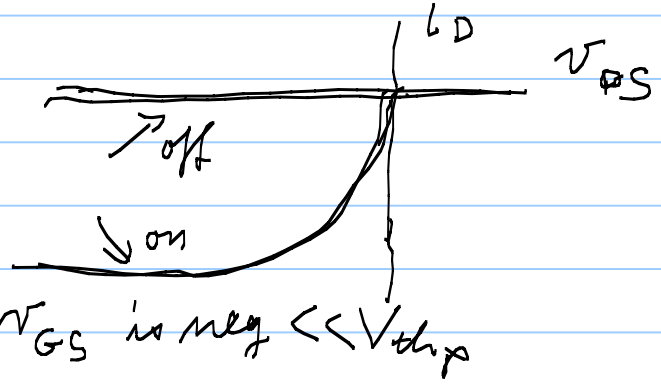
NMOS



$i_D = 0$ for $v_{GS} \leq V_{th}$



PMOS

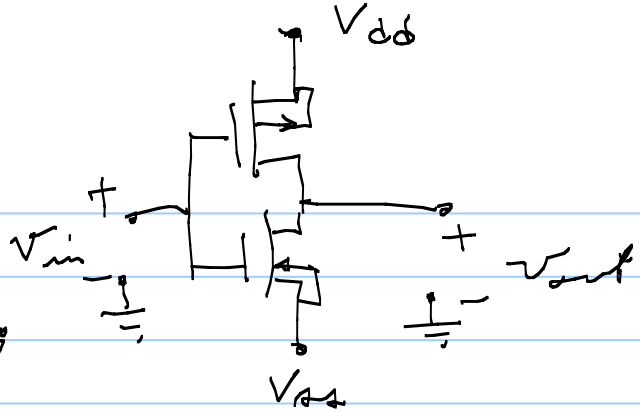


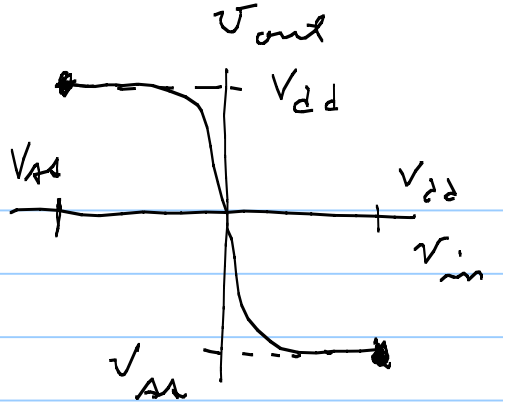
can make almost identicals when flip in origin by choosing W/L 's a

CMOS is for these satisfying

$i_{D_n} = -i_{D_p}$ when $v_{GS_n} = -v_{GS_p}$ & $v_{DS_n} = -v_{DS_p}$

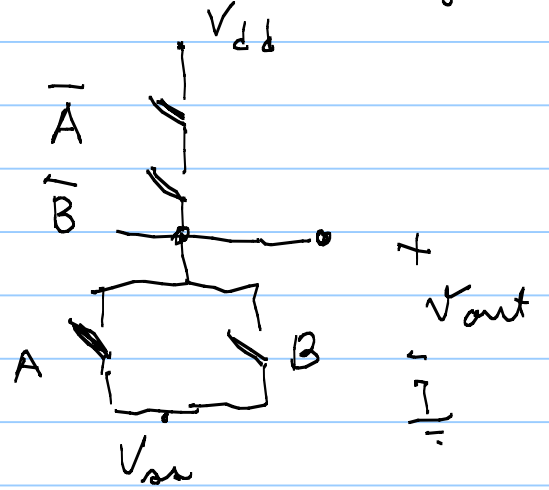
for the CMOS inverter
uses no power
unless are transitioning



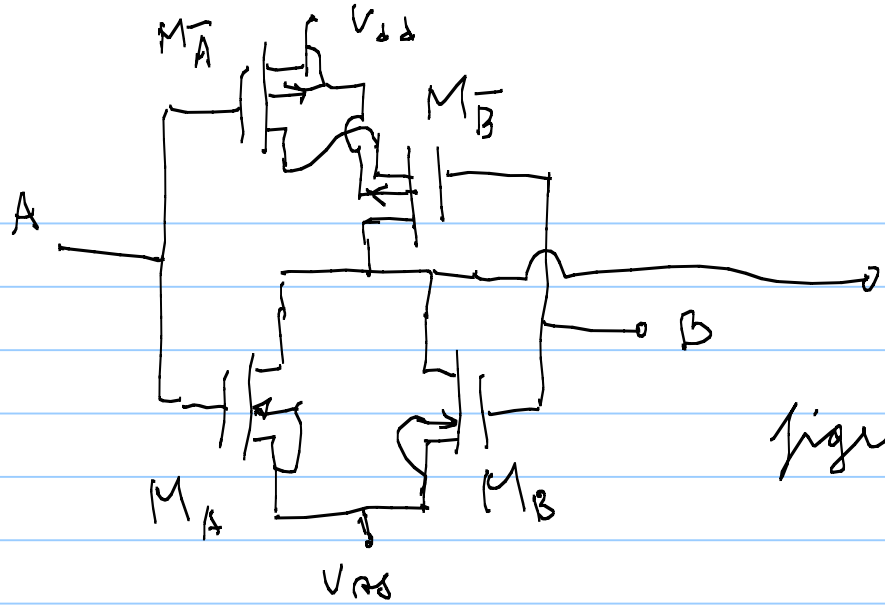


when $v_{in} = V_{dd}$, $v_{DS_n} = 0$ as $i_{D_n} \approx -i_{D_p} \equiv 0$

p. 967 = CMOS gates



if either A or B = 1 then $v_{out} = V_{ss}$
if both A & B = 0 then $v_{out} = V_{dd}$
1 = switch closed
0 = switch open
this is a nor gate

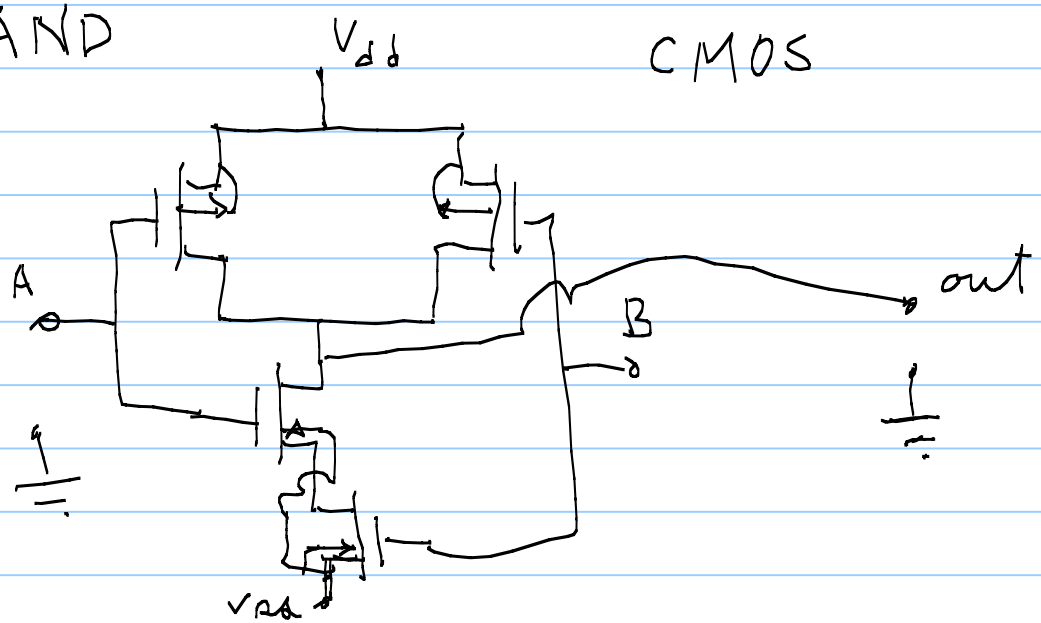


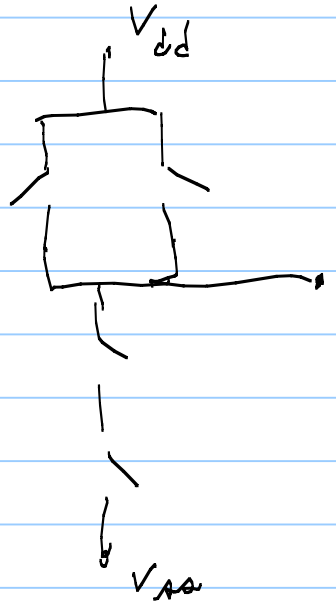
here $V_{th_p} \simeq V_{th_p}$ $M_{\bar{B}}$ $M_{\bar{A}}$

CMOS nor gate

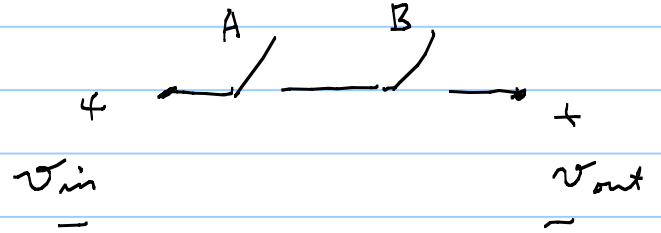
figure 10.12, p. 967

NAND CMOS

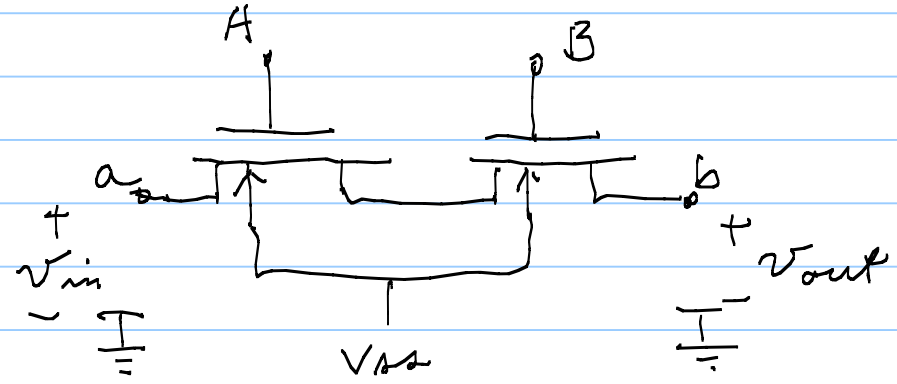




pass transistors — logic ⇒ PTL p. 983



$v_{out} = v_{in}$ if $A = B = 1$



if $v_{in} = v_a > v_b = v_{out}$
then a = drain
b = source

if $v_{in} = v_a < v_b = v_{out}$
then a = source
b = drain

;; can not tie bulks to either a or b or the middle
⇒ need to tie to V_{SS}