ENEE 417 - Spring 2003

Weeks #5 - #6

Design #2: CMOS Threshold Voltage Extractor and CMOS Curves

In this experiment a MOS circuit will be designed, constructed, and tested, that has as its output the threshold voltage of an MOS transistor.

1. Read the article: M. G. Johnson, "An Input-Free VT Extractor Circuit Using a Two-Transistor Differential Amplifier," IEEE Journal of Solid-State Circuits, Vol. 28, No. 6, June 1993, pp. 704-705.
2. Based on that paper design a threshold voltage extractor using the 4007 MOS transistors available in the Laboratory. Do Spice runs to check your design and construct and test your extractor. Consider the effects of different substrate voltages and means to handle both P and N MOS. For Spice computer runs note that the models to use are those of the equivalent RCA 3600 transistors in the PSpice model library CA3600.lib.
3. Display the results on the Tektronix oscilloscope and capture the oscilloscope display using the National Instruments GPIB bus controller.
4. Using LabView and the DAQ card save in the computer various graphs, including the MOS ID vs. VDS with VGS as a parameter and your VTO extractions. See P4.4 and P9.3 of the Textbook. Compare the transistor curves with those of PSpice.
5. Do a simulation of the circuit in PSpice using MOSIS 1.6 micron transistors (listed as 1.2 micron ones in the bicmos12 library). For that circuit do a VLSI layout of the VT extractor using MOSIS 1.6 micron technology (lambda=0.8 in MAGIC). Be sure to do a Spice extraction of your layout to check it versus
6. Write a short report summarizing your study.
7. Be sure to get your TA right away a parts list for your base paper so that items not on hand can be considered in time.