HOMEWORK − 3

ENEE −302

DUE DATE: 04/23/02 **DK**

Note: Only problems 1,2, and 4 will be graded.

1. Sketch a CMOS logic circuit that realizes the function $Y = A\,B + \overline{A}\ \overline{B}$. (20 pts)

2. A CMOS logic gate is required to provide an output $Y = \overline{A}\,B\,C + A\,\overline{B}\,C + A\,B\,\overline{C}$ .What is the minimum number of transistors used to realize this expression? Sketch Pull down network and Pull up network for realizing this expression. (30pts)

3. Sketch the CMOS logic circuit that realizes a two input NOR gate.

($Y = \overline{A + B}$)

4. A CMOS inverter has equivalent capacitance C = 50 fF, $k_n = 10\ k_p = 30?A/V^2$ $(W/L)_n=4?m/2?m$,$(W/L)_p= 10?m/2?m$. The supply voltage is 5V.Calculate the propagation delay for this inverter and also the dynamic power dissipated when the switching frequency is 100 MHz. (20 pts)