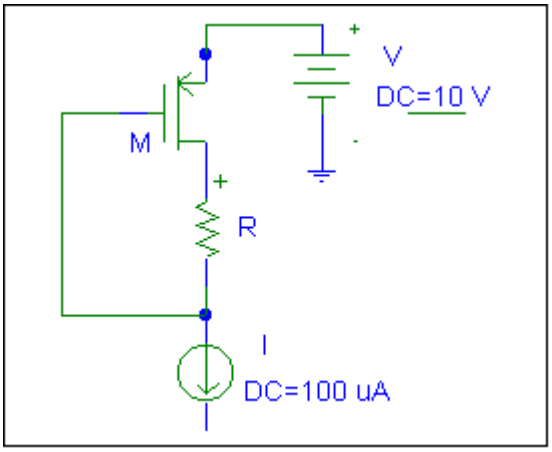
File: c:\course\spring2002\302\hmwrk4.doc WS/AD/RWN 04/29/02; revised 05/01/02

ENEE 302 Homework #4- revised

Work problems 1, 2, 4 & 6 for credit - due Tu May 7, 2002. Others are for practice and all represent possible topics for the final exam.

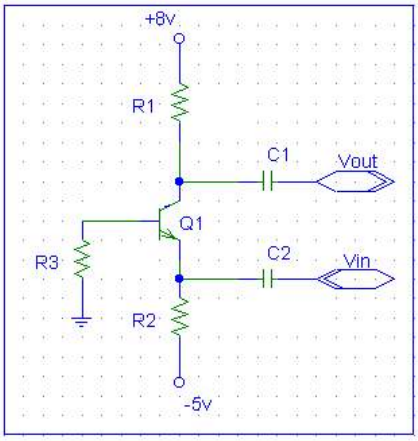
1. 30 points (WS) For the PMOS transistor in the circuit shown below, $k_p' = 8\ \mu A/V^2$, W/L = 25, and $|V_{tp}| = 1\,\text{V}$. For $I = 100\ \mu A$, find the voltages V_{SD} and V_{SG} for R = 0 and R =30 kΩ. For what value of R is $V_{SD} = V_{SG}/2$?



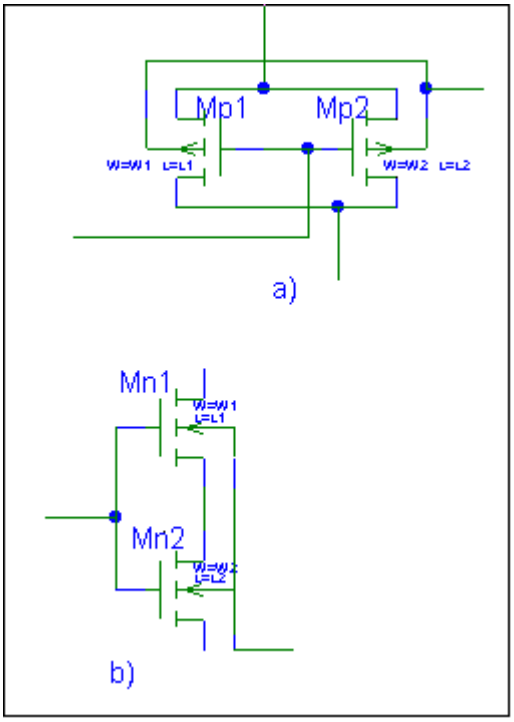
2. 35 points (AD) For the following common-base circuit:

a) Determine the gain Av(s) = Vout / Vin for all frequencies assuming Cμ=0.
b) Determine Zi and Zo, input and output impedances for all frequencies as functions of s. Calculate in terms of R1, R2, R3, C1 and C2 and assume no loading.
c) Plot Av(s) using PSpice and the BN2x2 npn transistor for R1= 3.6K, R2 = 3.9K, R3 = 390K, C1 = 5uF, C2 = 5uF.

Use the BN2x2 model parameters BF = 82, VAF=58 (check these in the Spice model). Assume Cπ much smaller than C1 and C2.



3. (RWN) Each of the following circuits is equivalent to one transistor. Assuming equal NMOS and equal PMOS transistors give the parameters for the equivalent transistors and label the nodes as to gate, drain, source and bulk.



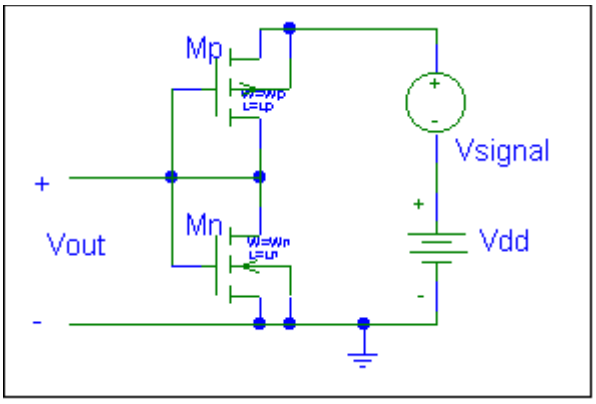
4. 30 points (RWN) For the translinear circuits presented on 04/25/02 replace the BJTs by NMOS. If these (NMOS) are biased by Ia=I1+I4 and Ib=I2+I3, express I1 as a function of I2. In the case that Ia=Ib discuss what this could be used for and if it has any advantage or disadvantage over other circuits which give the same function.

5. (RWN) In voltage mode the CMOS inverter of Fig. 13.4, p. 1050 of the text, is a convenient element for digital circuits. But for low voltage operation we prefer current mode. Using CMOS current mirrors design a current mode inverter. Give your design theory and do Spice simulations.

6. 35 points (RWN) For the following circuit

a) Assuming Vdd>Vthn+|Vthp| and Vsignal = 0 find Vout as a function of Vdd under no load conditions (for this determine the regions of operation of the transistors). Discuss how this circuit can be used to assist in biasing CMOS circuits; consider that at DC the gates of CMOS transistors do not draw current.

b) Assuming |Vsignal|<<Vdd find the transfer function Vout(s)/Vsignal(s) considering the presence of the Early effect (that is, the Spice parameter GAMMA >0).



7. (RWN) Use the BN2x2 and find its transition frequency f_T by doing a Spice frequency response (of short circuit collector current versus base current). Consider doing a comparable thing for an NMOS transistor.

8. Study CMOS flip-flops (what means D, J-K, S-R) and memory cells.