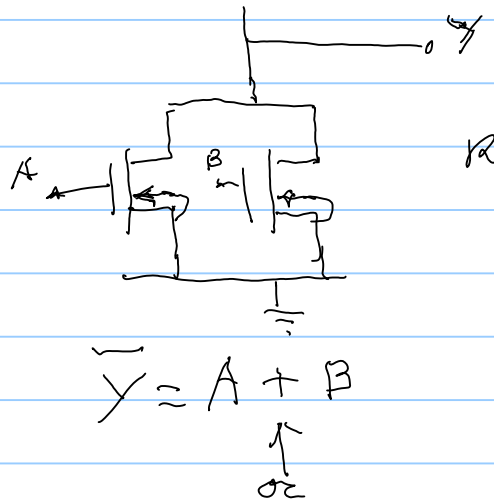
EE303H
11/08/16

Note Title 11/8/2016

Page 1093 = pull-up & pull-down CMOS

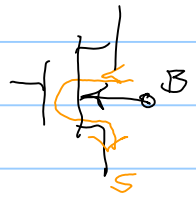


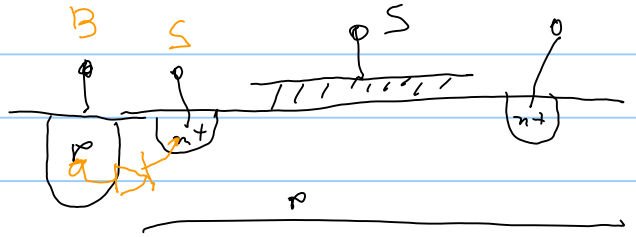
Pull down

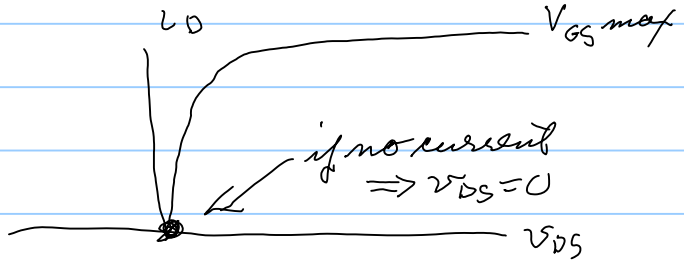
$\overline{Y} = A + B$

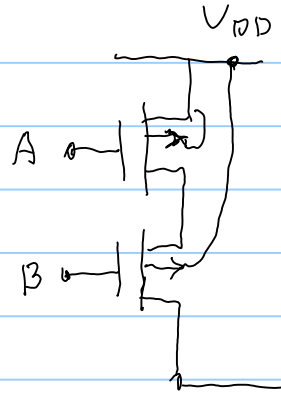
↑ or

and = · or = +





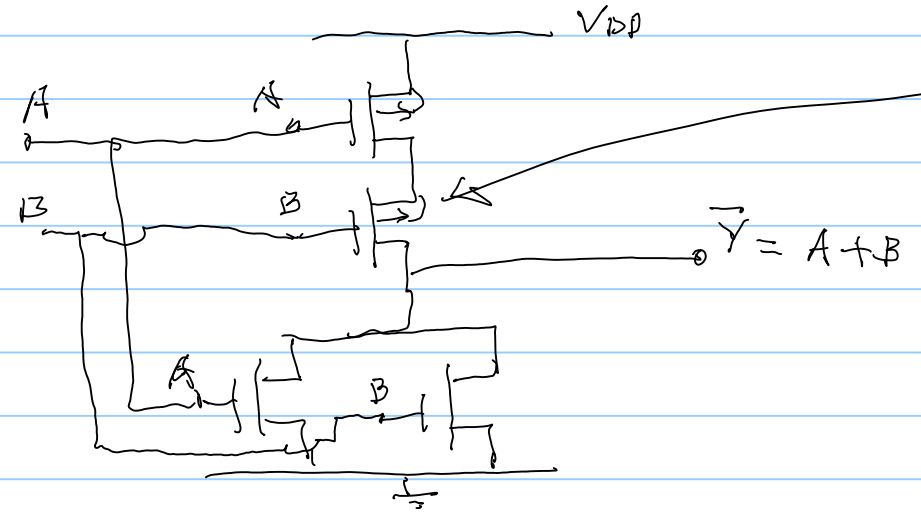




pull-up

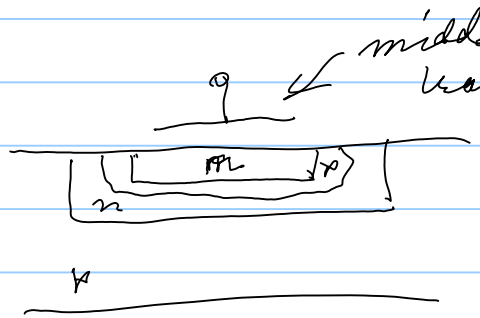
$$Y = \bar{A} \cdot \bar{B} \quad , \quad \bar{Y} = \overline{\bar{A} \cdot \bar{B}} = A + B$$

connected

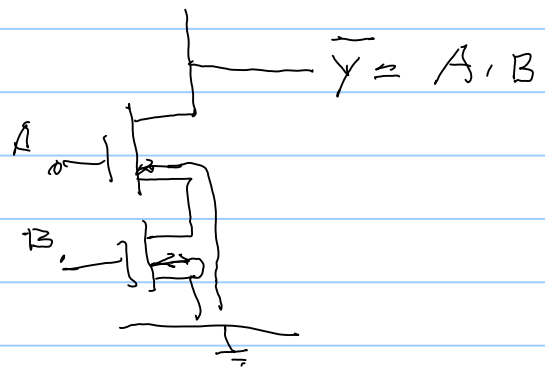


$\bar{Y} = A + B$

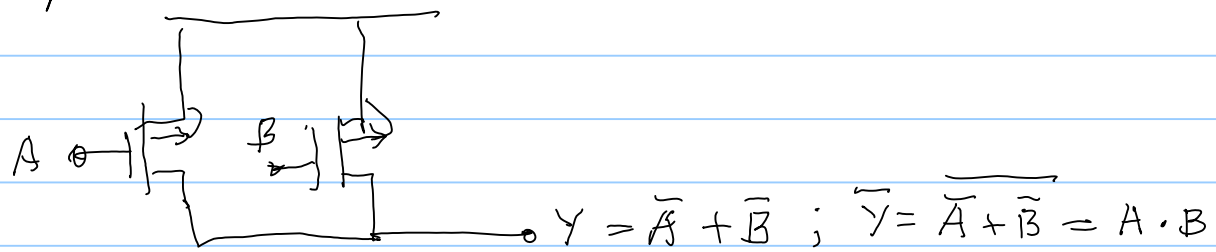
nor



Pull down

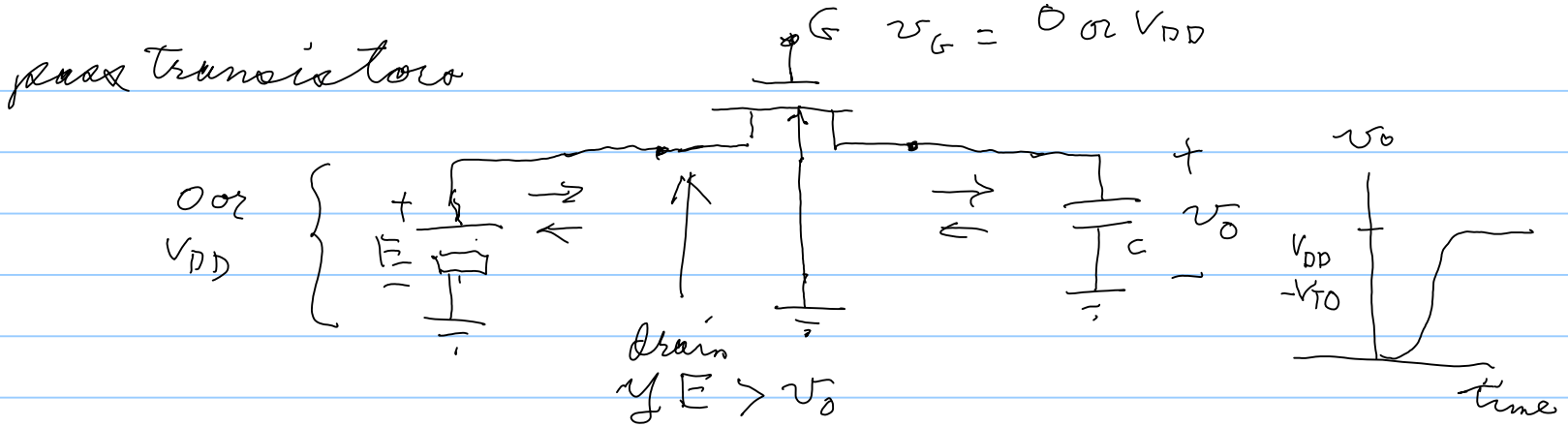


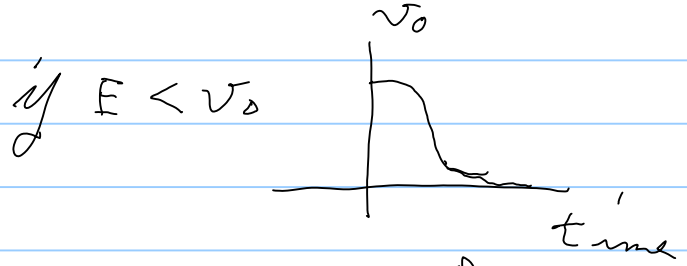
Pull up

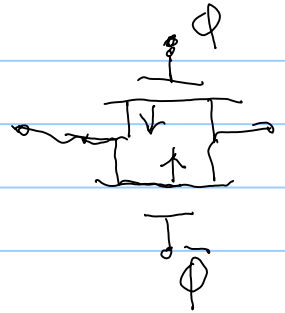


2 NAND gate
A
B
$\bar{B}$
$\bar{A}$
$\bar{Y} = A \cdot B$
V_{DD}
inverter connection
S
D
G

pass transistors

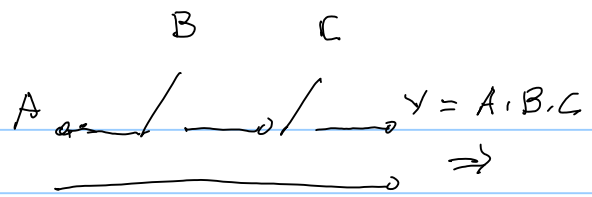


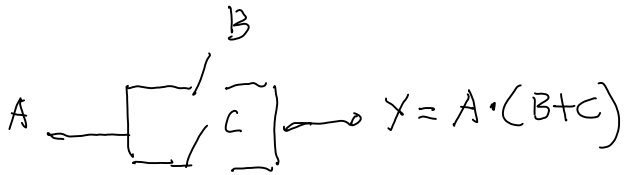




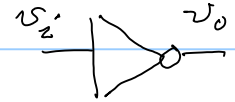
⇒ CMOS pass transistor Page 1193

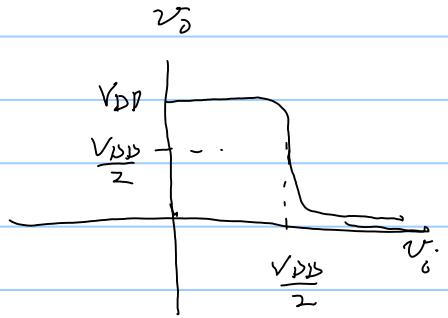
B_n at gnd B_p at V_{DD}

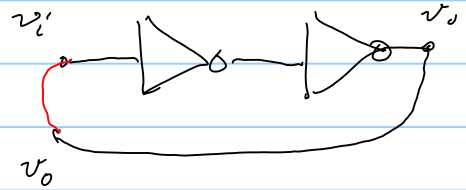


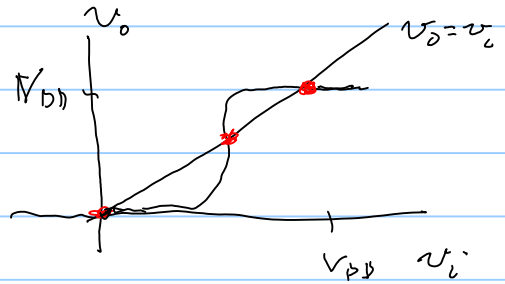


Latch, page 1239

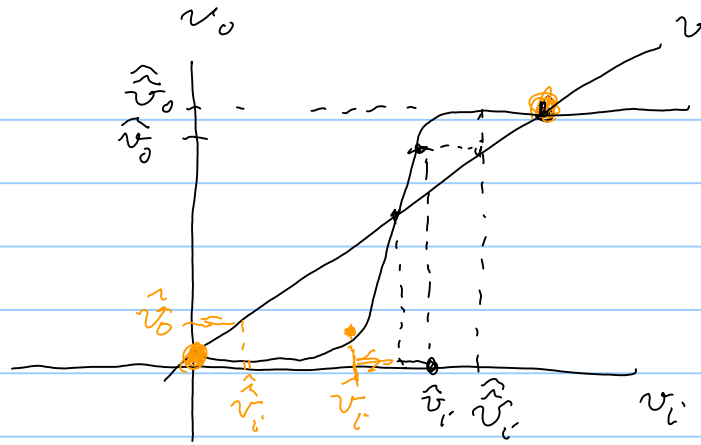






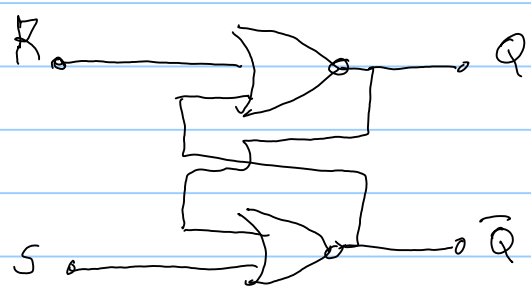


3 equilibrium point



stable set points

SR = set-reset flip flop



R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	not used