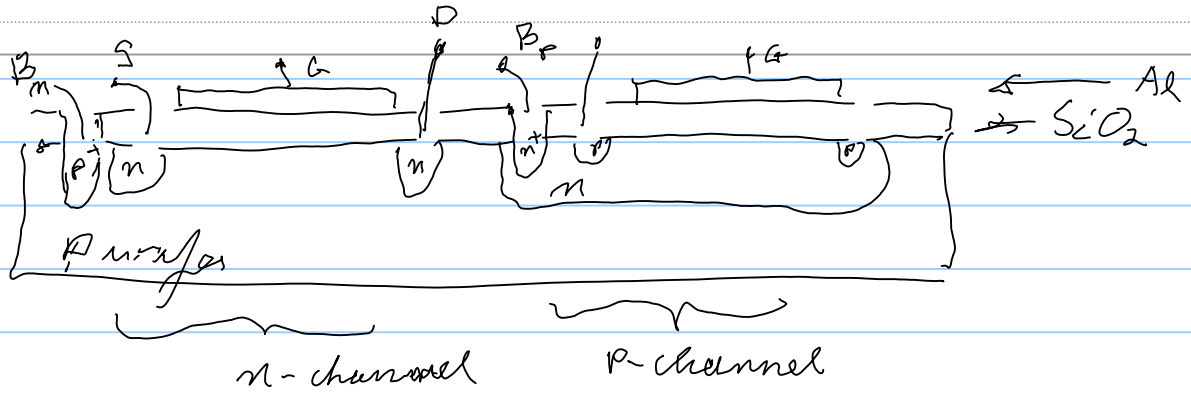
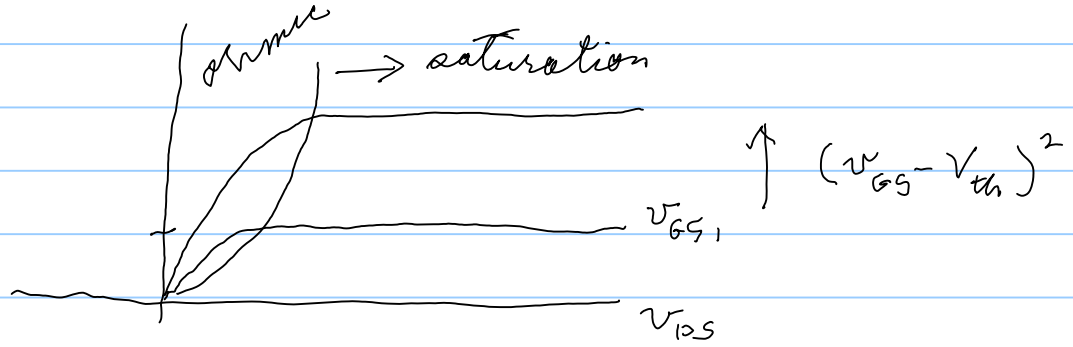
EE303H

10/04/16

Note Title 10/4/2016



B_n device at lowest potential on the chip } to back bias
B_p " " highest " " " " } source to bulk to
avoid bulk current



NMOS

$$V_{th} = VTO + \underbrace{\gamma}_{\text{GAMMA}} \left(\sqrt{\phi + v_{SB}} - \sqrt{\phi} \right)$$

can lowers V_{th} by $v_{SB} < 0$

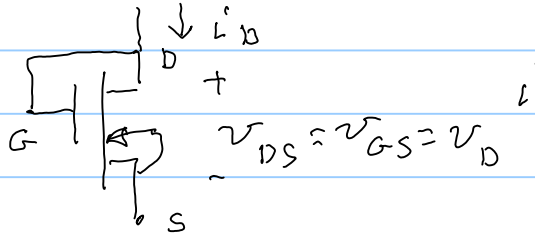
↑ gives the "body effect"

if $VTO_n > 0$ call the NMOS enhancement mode device

In saturation $i_{D_n} = \beta_n (v_{GS} - V_{th})^2 (1 + \lambda v_{DS})$

$$k_n = \frac{KP}{2} \cdot \frac{W}{L}$$

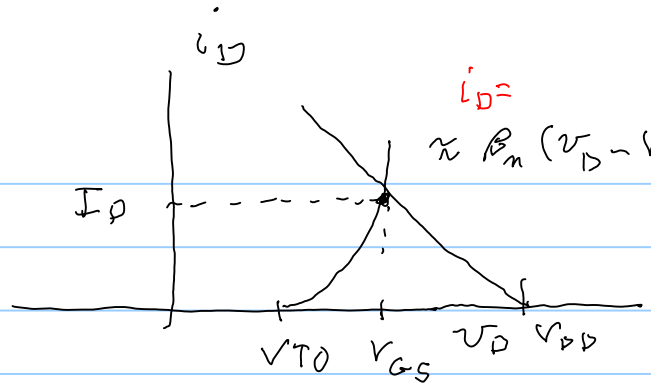
Look at a diode connected NMOS



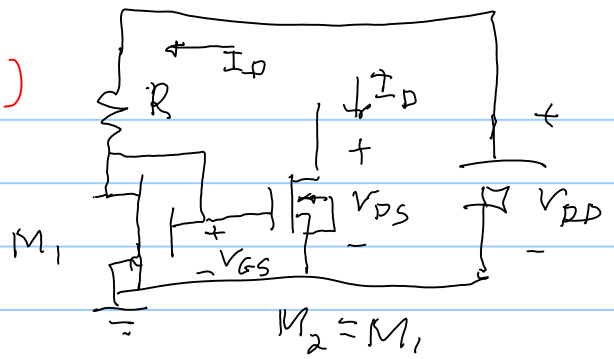
$$i_{D_n} = \beta_n (v_D - VTO)^2 (1 + \lambda v_D) \simeq \beta_n (v_D - VTO)^2$$

for $v_D > VTO$

if $0 \leq v_D < VTO$, $i_D = 0$

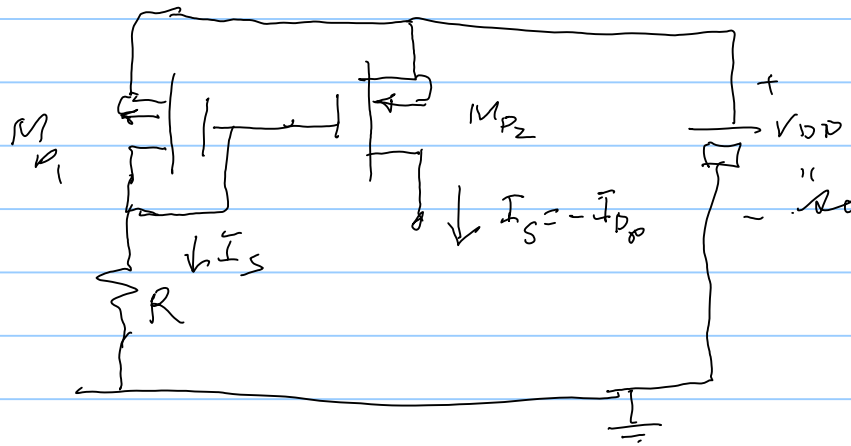


$$i_D = \approx \beta_n (v_D - V_{TO})^2 (1 + \lambda v_D)$$



$V_{DS} \geq V_{GS} - V_{TO}$

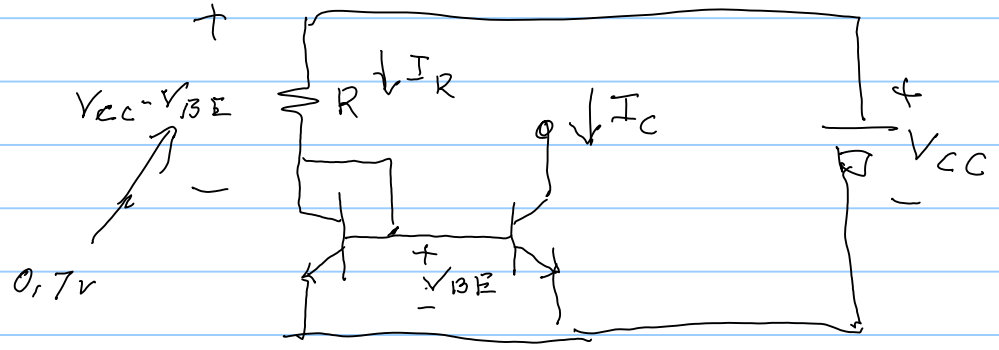
a current "sink"



"source" current

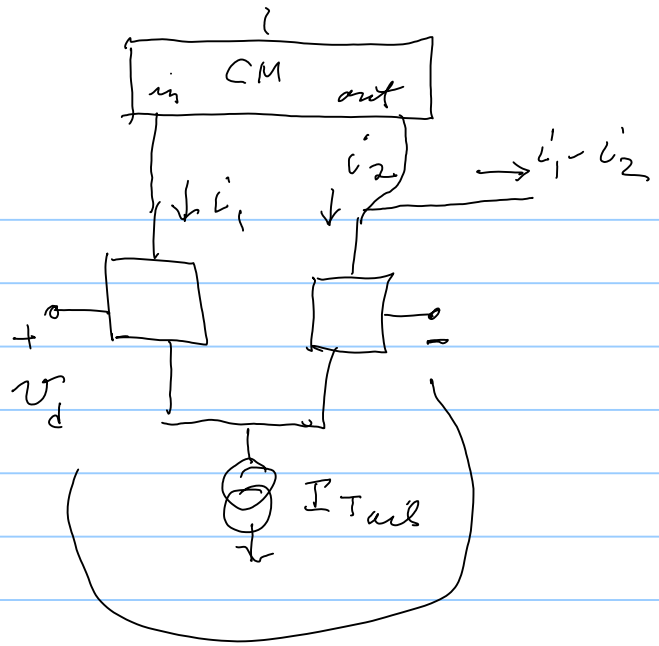
these are "bias" currents

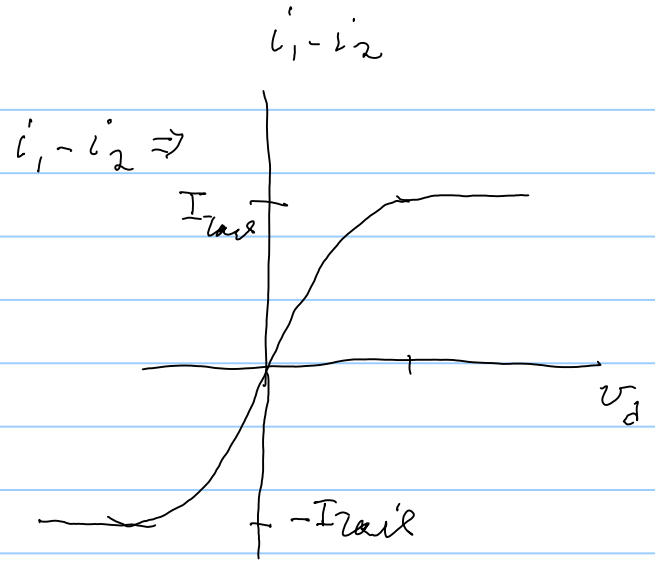
BJT version

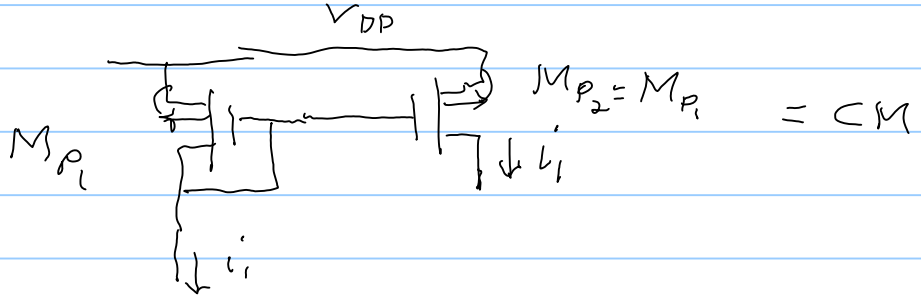


$$I_C \approx I_R = \frac{1}{R}(V_{CC}-V_{BE}) \Rightarrow R = \frac{V_{CC}-V_{BE}}{I_C}$$ gives design eq.

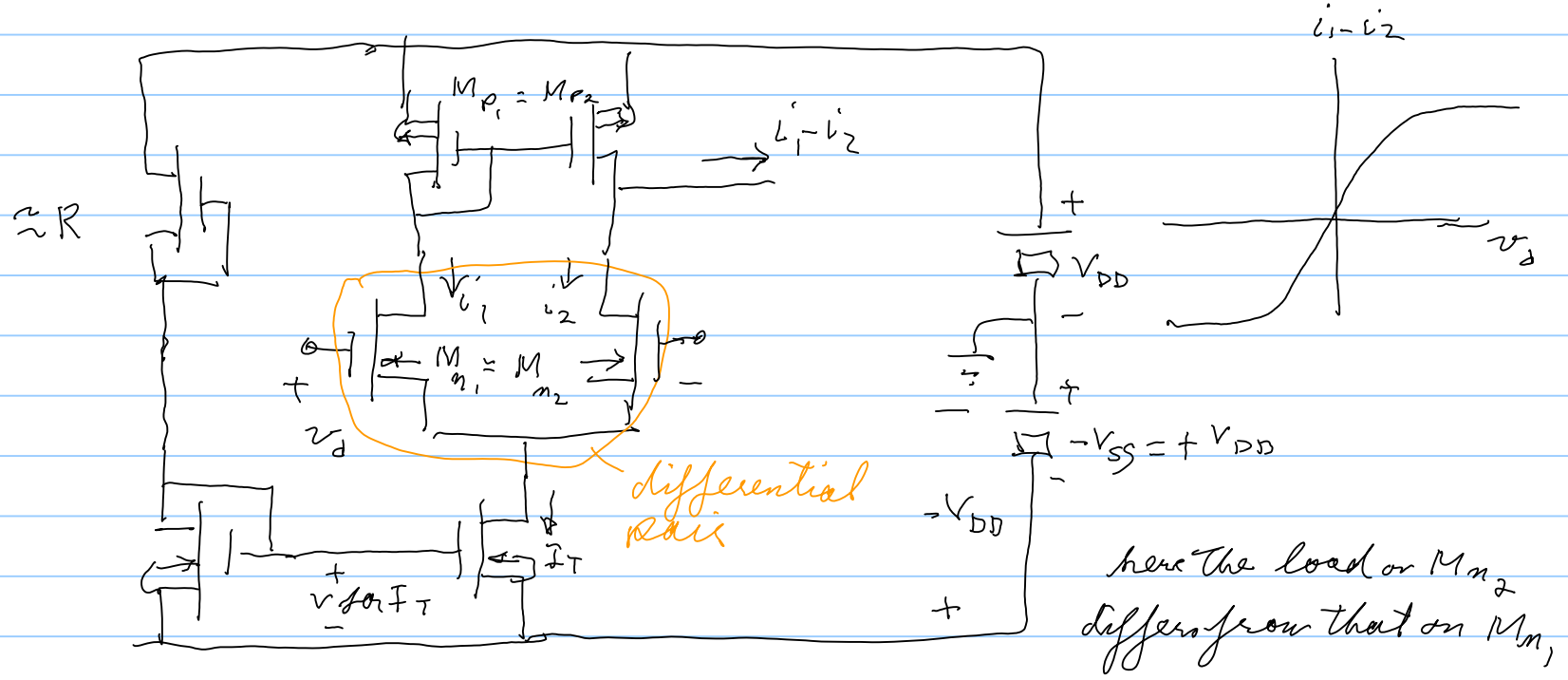
Differential pair


CM
in
out
i_2
$i_1 - i_2$
i_1
+
−
v_d
I_{Tail}

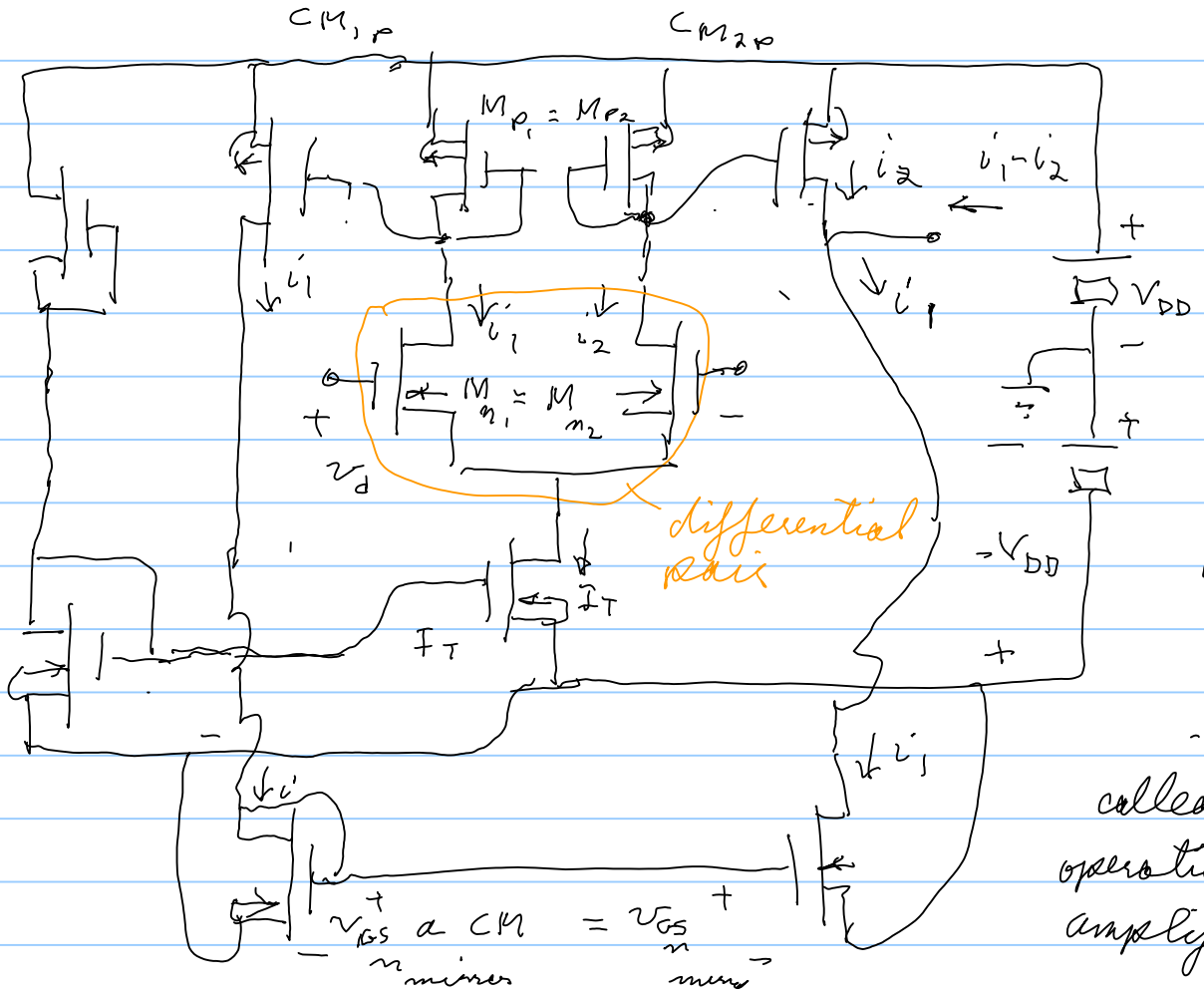

$i_1 - i_2$
$i_1 - i_2 \Rightarrow$
I_{Tail}
v_d
$-I_{Tail}$

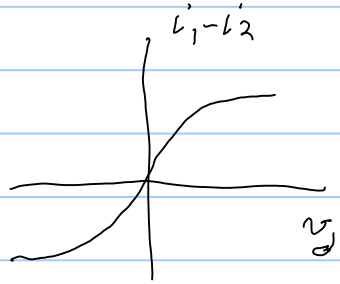

V_{DD}
$M_{P_2} = M_{P_1}$
M_{P_1}
i_1
i_1

$= CM$



here the load on M_{n_2} differs from that on M_{n_1}





if MOS $\Rightarrow$ BJT

$$i_d' = i_1' - i_2' = I_T \tanh\left(\frac{v_d}{2V_T}\right)$$

called an OTA
operational transconductance
amplifier