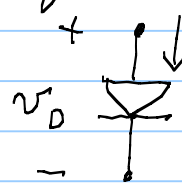
EE 303 H
09/04/14

Note Title 9/6/2014

Rewrite; class computer system down

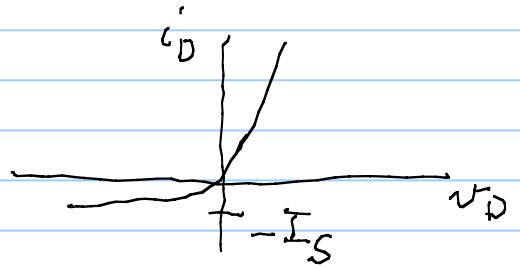
diode eq.; p. 150, eq. (3.40)
load line, p. 180, Fig. 4.11
small signal, p. 184, Fig. 4.13

pn junction diode

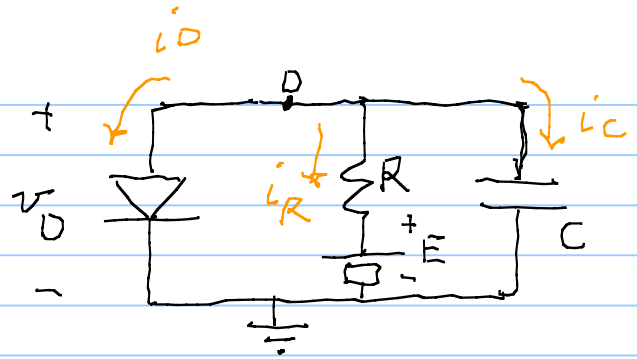


$i_D = I_S(e^{v_D/V_T} - 1)$

$V_T = kT/|q|$, q = electron charge
$= 0.026$ V @ room T



In a circuit



$$i_D = f(v_D) = I_S(e^{v_D/V_T} - 1)$$

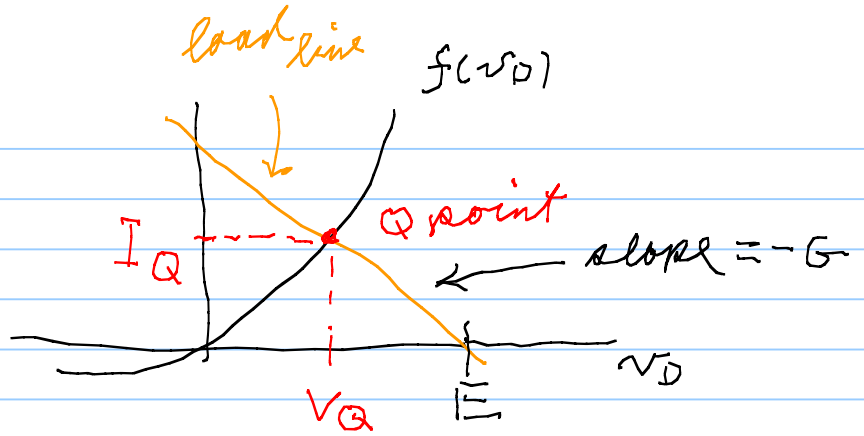
$$G = 1/R$$

KCL at node D: $0 = i_D + i_R + i_C \Rightarrow 0 = f(v_D) + G(v_D - E) + C\, dv_D/dt$

$$\Rightarrow C\frac{dv_D}{dt} = -G(v_D - E) - f(v_D)$$

at DC (= bias), $dv_D/dt = 0$ & $v_D \Rightarrow V_D = V_Q$, Q = quiescent

$\therefore$ @ bias $\quad f(v_D) = -G(v_D - E)$



— = right side eq.
$i' = -G(v_D - E)$

— = left side, device eq.
$i = f(v_D)$

For small signal, expand in Taylor series about $v_D = V_Q$

$\therefore$ need $di_D/dv_D = \left.\frac{d\, I_S e^{v_D/V_T}}{dv_D}\right|_{V_Q} = \frac{I_S}{V_T} \cdot e^{V_Q/V_T} \triangleq g_D$ = slope of diode curve @ Q

if in $v_D > 0$ region $i_D \simeq I_S e^{v_D/V_T}$ & $\frac{di_D}{dv_D} \simeq \frac{i_D}{V_T} \Rightarrow g_d \simeq \frac{I_D}{V_T} \simeq \frac{I_Q}{V_T}$

∴ The expansion for the circuit needs

needs $i_D = f(v_D) = f(V_Q) + \left.\frac{df}{dv_D}\right|_{V_Q}(v_D - V_Q) + \frac{1}{2}\left.\frac{d^2 f}{dv_D^2}\right|_{V_Q}(v_D - V_Q)^2 + \cdots$

ignore if $(v_D - V_Q)$ is small

$\therefore \; i_D \simeq I_Q + g_d(v_D - V_Q)$

expanding KCL terms about $v_D = V_Q$

$$C\frac{dv_D}{dt} = C\frac{d(v_D - V_Q)}{dt} \quad (\text{as } dV_Q/dt = 0)$$

$$= -G(v_D - V_Q) - \left\{I_Q + g_d(v_D - V_Q)\right\}$$

Let $v_d = v_D - V_Q = v_D - V_D \equiv v_D = V_D + v_d$

v_D: total, V_D: bias, v_d: signal

gives $C\,dv_d/dt = -G(\underbrace{v_D - V_Q}_{v_d} + V_Q - E) - \{I_Q + g_d \cdot v_d\}$

$$\Rightarrow \quad C\,dv_d/dt = -I_Q + G(E - V_Q) - G v_d - g_d \cdot v_d$$

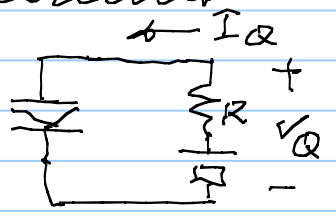
Separate bias (= DC ⇒ constant) terms & changing (= signal) terms

bias: $0 = -I_Q + G(E - V_Q) \Rightarrow I_Q = G(E - V_Q)$

signal: $C\,dv_d/dt = -G v_d - g_d v_d \Rightarrow C\dot{v}_d + (g_d + G) v_d = 0$

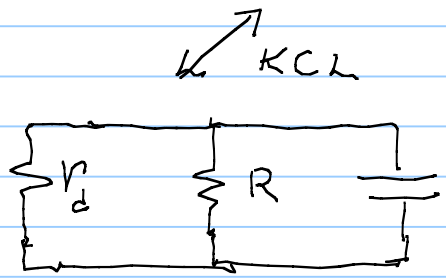
gives 2 circuits

bias



small signal

KCL



$r_d \simeq 1/g_d$

∴ the circuit design problem with transistors will involve two circuits, the bias one and the signal one. Since g_d depends on V_Q the two problems intertwine and one needs to choose the Q point with signal in mind.