303H Fall 2014 – Homework 7 Due Th 10/23/14

1. (60 points, inverter properties)
    Consider a CMOS inverter using Vdd=-Vss=9v made of bicmos transistors.
    a) Assume the NMOS transistor has W=L=20u. If the PMOS L=20u, find the PMOS W such that 0V in gives 0V out.
    b) Check the result of a) in Spice and adjust the PMOS W so the actual ouput is 0V when the input one is 0V. Comment upon the result.
    c) With the adjusted inverter of b) run and submit the Vout versus Vin DC curve.
    d) Excite with a voltage pulse input from 0 to Vdd with different rise times and check the output rise time (and shape).
    e) Obtain a frequency response for Vout/Vin by doing an AC Spice run from 10Hz to 1GHerz. When biased at Vout=0 when Vin=0, the circuit supposedly acts as a linear analog amplifier. Check its DC small signal gain.

2. (40 points, 3 cascade inverters with feedback)
    [note: To get Spice to give non-zero results you can excite with a short pulse of current]
    a) Connect in cascade three of the inverters of the above problem part b) with feedback from the third stage output to the first stage input. Do a Spice transient analysis and calculate the pulse repetition rate of Vout(t). Explain the results.
    b) Set Vss=0 and repeat. Then reset Vss = -9V but set Vdd=0 and repeat. Comment on any differences.