File: G:/coursesF14/303H/303HF14Final.doc RWN 12/07/14

ENEE 303H Final Exam – Fall 2014

Take Home; due 10am M 12/15; classroom – Signature certifies that all the work is your own

150 points, 2 hours, open book, open notes. Notebooks are due at the end of the exam.

Good luck and have a good semester break

.

1. (50 points, 30 minutes)

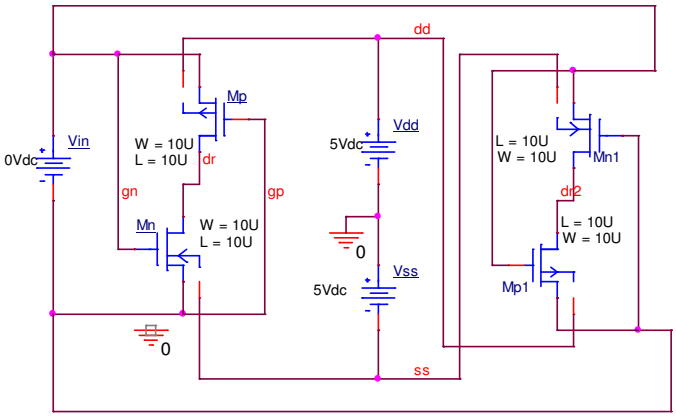
The following circuit uses the Wilamowski resistor, on the left, with its complement, on the right, to make a bilateral resistor.

a) Make an analytic analysis of the DC behavior of the resistor on the left (made of Mn and Mp with leads fed by Vin) to give its Iin as a function of Vin, Iin=f(Vin)=-I(Vin), for 0≤Vin≤Vdd. Assume that Mp is completely complementary to Mn.

b) Obtain Spice curves for the following circuit using MNMOSIS and MPMOSIS transistors. Run for –Vdd≤Vin≤Vdd.

c) Compare the Spice results with the theoretical Iin=f(vin).

d) Attach the floating ground to the source of Mn and discuss the problem that occurs.



Reference: Y. Ota and B. M. Wilamowski, "CMOS Implementation of a Voltage-Mode Fuzzy Min-Max Controller," Journal of Circuits, Systems, and Computers, Vol. 6, No. 2, pp. 171-184, April, 1996.

2. (50 points, 30 minutes)

This problem uses the standard CMOS working between ground and Vdd.

a) The formula for the value, V_M, of Vin when Vout=Vin ($=V_M$) as given on the web by Professor Paul A. Morton at Michigan State for ECE 410 Lecture note 7.5 is

$$V_M = \frac{Vdd - |V_{tp}| + V_{tn}\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}}$$

Give the conditions under which this is true.

b) If the Early effect is considered, the above formula changes and requires solution of a cubic equation. But when the Early voltage is large, $\lambda<<1$, solving the cubic can be avoided by simply modifying the above equation using the approximations $1/(1+x)=1-x$ and $\sqrt{(1+x)}=1+x/2$. Use these approximations to give an improved equation for V_M.

c) Evaluate V_M for the CMOS 4007 transistors using Vdd=6V first when $\lambda=0$ and then when $\lambda\neq 0$ and compare. The Spice models for these are on the course web page.

3. (50 points, 20 minutes)

The following NMOS transistor works in sub-threshold for which the law is

$$I_D = I_S e^{V_{GS}/nV_T}(1-e^{-V_{DS}/V_T})$$

where V_T=thermal voltage=0.026V, n=3, I_S=saturation current=20E-18 (includes other factors such as VTO).

a) Find the small signal conductance g=dI/dV when biased at $V_b>0$.

b) This circuit is claimed to give very large resistance for small signals. Determine if this is the case when it is biased at V_b=0.6V.

c) What happens if V<0 ?